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(54) A modifiable circuit, methods of use and making thereof

(57) A modifiable circuit for modifying a revision identifier (ID) or default register value, and for coupling at least two adjacent logic blocks in an integrated circuit chip, and methods for manufacturing the same. The circuit comprises a memory cell, a register and a control circuit. The memory cell, which may be termed a "Meta-Memory Cell" (MMCEL), has a first metal interconnect structure that traverses the plurality of metal layers using a first plurality of vias, wherein the first metal interconnect structure is located at a boundary of the at least two adjacent logic blocks. The memory cell also has a second metal interconnect structure that traverses the plurality of metal layers using a second plurality of vias, wherein the second metal interconnect structure is located at the boundary of the at least two adjacent logic blocks. The interconnect is formed between the at least two adjacent logic blocks by at least one of the first and second metal interconnect structures, wherein a state of the interconnect is programmable by altering any one of the plurality of metal layers or any one of a plurality of via layers. The register has a data input, a data output and control inputs. The control circuit is coupled to the control inputs of the register. The control circuit receives a chip reset signal and the memory cell output to thereby force the data output of the register to a default register value that equals the output of the memory cell, regardless of the data input of the register.

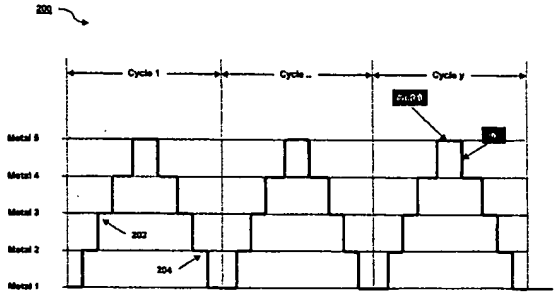


FIG. 2

Description

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] The present invention is directed to integrated circuit (IC) chips, and more particularly to revision identification (ID) number modification; default register values in an IC modification; and to coupling of power, control and data signals between adjacent functional blocks in an IC using a modifiable circuit.

Related Art

[0002] An embodiment of the present invention provides a solution to a problem that plagues conventional integrated circuit (IC) chips. The problem is the hidden cost of additional metal mask layers when implementing a revision identification (ID) of the chip. This is a necessary requirement in order to inform a customer through software that the existing design of the chip has changed.

[0003] Conventionally, the revision ID is implemented as bits that are tied to either VDD (supply) or GND (ground) at any arbitrary layer of the chip. An additional metal layer is consumed by the revision ID when actual design changes are made on a different metal layer than where the revision ID was originally connected. For example, an additional metal layer will be consumed if the chip requires a logic fix on the metal 2 layer and the next revision ID bit needs to be tied to GND (ground) on the metal 4 layer. This will require two metal mask layer changes instead of just one on the metal 2 layer. Modification to the metal 4 layer is not necessary if the Revision ID could be changed in the metal 2 layer. In 0.18μm technology, the cost per metal layer is high, and in 0.13 μm technology, the cost is even higher. Hence, the cost increases for finer pitch technology.

[0004] Additional costs also result from the engineering hours spent on the laborious layout task of minimizing the number of metal layers used to implement a change in the revision ID. For example, this task may consume a number of days just to save a metal mask. In addition, completely unique designs must be implemented for each chip in order to save mask costs. As a result, these designs cannot be re-used for other projects.

[0005] Significant cost savings for a company can be attained if one could completely eliminate the waste of mask layers and extra labor due to revision ID bit changes. This is a problem that affects a vast number of conventional IC chips.

[0006] Modifiable revision ID schemes exist, such as those described in U.S. Patent Nos. 5,590,069 and 5,644,144, which are incorporated by reference herein in their entirety. The schemes disclosed in these two patents suffer from inefficient topological layouts.

BRIEF SUMMARY OF THE INVENTION

[0007] One embodiment of the present invention is directed to a modifiable circuit for coupling at least two adjacent logic blocks in an integrated circuit chip, wherein the chip includes a plurality of metal layers, and first and second power supply potentials. The circuit comprises a first and second metal interconnect structures, and an interconnect. The first metal interconnect structure traverses the plurality of metal layers using a first plurality of vias, wherein the first metal interconnect structure is located at a boundary of the at least two adjacent logic blocks. The second metal interconnect structure traverses the plurality of metal layers using a second plurality of vias, wherein the second metal interconnect structure is located at the boundary of the at least two adjacent logic blocks. The interconnect is formed between the at least two adjacent logic blocks by at least one of the first and second metal interconnect structures, wherein a state of the interconnect is programmable by altering any one of the plurality of metal layers or any one of a plurality of via layers. The first metal interconnect structure can be coupled to one of the first and second supply potentials and the second metal interconnect structure is coupled to the other one of the first and second supply potentials. Prior to programming, the first and second metal interconnect structures can be coupled at a top metal layer.

[0008] In another embodiment, multiples of the first and second metal interconnect structures are coupled together to form a plurality of modifiable cycles, wherein each half cycle is modifiable at least once. In an alternative implementation, one cycle can be laid-out to form a ladder structure that traverses the plurality of metal layers from a bottom metal layer to a top metal layer and back to the bottom metal layer. The ladder structure can be arranged to form a cube-shaped structure. In this arrangement, the first and second supply potentials can comprise two buses located in a central region of the cube-shaped structure and are accessible at each of the metal layers. Alternatively, the ladder structure can be arranged to form a spiral-shaped structure. In this other arrangement, the first and second supply potentials can comprise buses accessible at each of the metal layers.

[0009] Another embodiment of the present invention is directed to a method of making a programmable memory cell for storing a value in an integrated circuit chip. The chip includes first and second supply potentials. The method comprising forming a plurality of metal layers separated by a plurality of via layers, including a first metal interconnect structure that traverses the plurality of metal layers using a first plurality of vias in the plurality of via layers. A second metal interconnect structure is formed, which traverses the plurality of metal layers using a second plurality of vias in the plurality of via layers. The first and second metal interconnect structures are coupled together at a top metal layer prior to programming. Additionally, one of the first and second supply

potentials are coupled to at least one of the first and second metal interconnect structures to form an output. At least one of the plurality of metal layers is then altered to thereby program the output. Multiples of the first and second metal interconnect structures can be formed and coupled together to form a plurality of programmable cycles for the memory cell, wherein each half cycle is programmable at least once.

[0010] A one-cycle ladder structure can be formed that traverses the plurality of metal layers from a bottom metal layer to a top metal layer and back to the bottom metal layer. The ladder structure in a shape of a cube or a spiral. The first and second supply potentials can be formed as two buses located in a central region of the cube-shaped structure and so as to be accessible at each of the metal layers. Alternatively, the first and second supply potentials can be formed as buses accessible at each of the metal layers in the case of the spiral embodiment. By altering any one of the plurality of metal layers and/or any one of the via layers, the memory cell can be reprogrammed repeatedly. The programming is reversible during any subsequent chip revision.

[0011] The memory cells of the present invention can be inserted into subsequent versions of previously designed chips. For example, chips that have been fabricated and whose base layers are already fixed can receive the memory cells of the present invention during an all-metal change provided that sufficient chip space is available. This drop-in compatibility permits chip designers to enable or disable logic fixes in one metal or one via layer through use of memory cells of the present invention, which can reduce design risks due to cost.

[0012] In yet another embodiment of the present invention, a memory cell circuit for modification of a default register value in an integrated circuit chip is disclosed, which includes a plurality of metal layers and first and second supply potentials. The circuit comprises a memory cell, a register and a control circuit. The memory cell has a first metal interconnect structure that traverses the plurality of metal layers using a first plurality of vias, wherein the first metal interconnect structure is coupled to one of the first and second supply potentials, a second metal interconnect structure that traverses the plurality of metal layers using a second plurality of vias, wherein the second metal interconnect structure is coupled to the other one of the first and second supply potentials, and an output, wherein a state of the output is programmable by altering any one of the plurality of metal layers or any one of a plurality of via layers. The register has a data input, a data output and control inputs. The control circuit is coupled to the control inputs of the register. The control circuit receives a chip reset signal and the memory cell output to thereby force the data output of the register to a default register value that equals the output of the memory cell, regardless of the data input of the register.

[0013] The control circuit can be implemented using logic gates, such as a first and a second NAND gate and an inverter. The chip reset signal can be input to the first and second NAND gates, the memory cell output input to the second NAND gate and the inverter. In this manner, an output of the inverter is input to the first NAND gate, and outputs of the first and second NAND gates are provided to the control inputs of the register. The register can comprises a flip-flop, such as a D-Q flip-flop.

[0014] In one embodiment, prior to programming, the first and second metal interconnect structures are coupled at a top metal layer. Alternatively, the circuit can have multiples of the first and second metal interconnect structures coupled together to form a plurality of programmable cycles for the memory cell, wherein each half cycle is programmable at least once. One cycle can be laid out to form a ladder structure that traverses the plurality of metal layers from a bottom metal layer to a top metal layer and back to the bottom metal layer. The ladder structure can be arranged to form a cube-shaped structure. In this configuration, the first and second supply potentials can comprise two buses located in a central region of the cube-shaped structure and are accessible at each of the metal layers. Alternatively, the ladder structure can be arranged to form a spiral-shaped structure, in which the first and second supply potentials comprise buses accessible at each of the metal layers. Each of the first and second metal interconnect structures can be reprogrammed repeatedly by altering any one of the plurality of metal layers. Moreover, each of the first and second metal interconnect structures can be reprogrammed repeatedly by altering any one of a plurality of via layers. In a still further implementation , each of the first and second metal interconnect structures can be reprogrammed repeatedly by altering any one of the plurality of metal layers and any one of a plurality of via layers.

[0015] Dual outputs for the memory cell are achieved by not electrically coupled the first and second metal interconnect structures to each other at a top metal layer. In this and other arrangements, one of the first and second metal interconnect structures is coupled to the first supply potential at a bottom metal layer and the other of the first and second metal interconnect structures is coupled to the second supply potential at the bottom metal layer.

[0016] In still another embodiment, the first and second metal interconnect structures are arranged to from a ladder structure that can be arranged to from an offset ladder structure or a stacked structure. The stacked structure comprises first and second alternating metal interconnect patterns. The stacked can comprise a first alternating metal interconnect pattern having first and second interspersed metal traces, and a second alternating metal interconnect pattern having third and fourth interspersed metal traces, wherein the third and fourth interspersed metal traces form a mirror image of first and second interspersed metal traces. The first plurality

of vias can interconnect ones of the first and third interspersed metal traces and the second plurality of vias can interconnect ones of the second and fourth interspersed metal traces. In this and other arrangements, the memory cell can be programmed at any metal layer by forming an open circuit in each of the first and second interspersed metal traces of that layer thereby splitting each metal trace into two portions, and coupling together a first portion of the first interspersed metal trace to a first portion of the second interspersed metal trace and coupling together a second portion of the first interspersed metal trace to a second portion of the second interspersed metal trace.

[0017] Programmed at any of a plurality of via layers can be performed by removing two vias and inserting two vias. The programming is reversible during a subsequent chip revision.

[0018] In yet still another embodiment, one of the first and second metal interconnect structures is coupled to the first supply potential at a bottom metal layer and the other of the first and second metal interconnect structures is coupled to the second supply potential at the bottom metal layer.

[0019] The memory cells of the present invention can be inserted into subsequent versions of previously designed chips. For example, chips that have been fabricated and whose base layers are already fixed can receive the memory cells of the present invention during an all-metal change provided that sufficient chip space is available. This drop-in compatibility permits chip designers to enable or disable logic fixes in one metal or one via layer through use of memory cells of the present invention, which can reduce design risks due to cost.

[0020] Another embodiment of the present invention is directed to a modifiable circuit for coupling at least two adjacent logic blocks in an integrated circuit chip, wherein the chip includes a plurality of metal layers, and first and second power supply potentials. The circuit comprises a first and second metal interconnect structures, and an interconnect. The first metal interconnect structure traverses the plurality of metal layers using a first plurality of vias, wherein the first metal interconnect structure is located at a boundary of the at least two adjacent logic blocks. The second metal interconnect structure traverses the plurality of metal layers using a second plurality of vias, wherein the second metal interconnect structure is located at the boundary of the at least two adjacent logic blocks. The interconnect is formed between the at least two adjacent logic blocks by at least one of the first and second metal interconnect structures, wherein a state of the interconnect is programmable by altering any one of the plurality of metal layers or any one of a plurality of via layers. The first metal interconnect structure can be coupled to one of the first and second supply potentials and the second metal interconnect structure is coupled to the other one of the first and second supply potentials. Prior to programming, the first and second metal interconnect structures can be coupled at a top metal layer.

[0021] In another embodiment, multiples of the first and second metal interconnect structures are coupled together to form a plurality of modifiable cycles, wherein each half cycle is modifiable at least once. In an alternative implementation, one cycle can be laid-out to form a ladder structure that traverses the plurality of metal layers from a bottom metal layer to a top metal layer and back to the bottom metal layer. The ladder structure can be arranged to form a cube-shaped structure. In this arrangement, the first and second supply potentials can comprise two buses located in a central region of the cube-shaped structure and are accessible at each of the metal layers. Alternatively, the ladder structure can be arranged to form a spiral-shaped structure. In this other arrangement, the first and second supply potentials can comprise buses accessible at each of the metal layers.

[0022] In an embodiment, each of the first and second metal interconnect structures can be reprogrammed repeatedly by altering any one of the plurality of metal layers.

[0023] In another embodiment, each of the first and second metal interconnect structures can be reprogrammed repeatedly by altering any one of a plurality of via layers.

[0024] In still a further embodiment, each of the first and second metal interconnect structures can be reprogrammed repeatedly by altering any one of the plurality of metal layers and any one of a plurality of via layers. One of the first and second metal interconnect structures is coupled to the first supply potential at a bottom metal layer and the other of the first and second metal interconnect structures is coupled to the second supply potential at the bottom metal layer to provide a dual output arrangement.

[0025] The memory cells of the present invention can be inserted into subsequent versions of previously designed chips. For example, chips that have been fabricated and whose base layers are already fixed can receive the memory cells of the present invention during an all-metal change provided that sufficient chip space is available. This drop-in compatibility permits chip designers to enable or disable logic fixes in one metal or one via layer through use of memory cells of the present invention, which can reduce design risks due to cost.

According to an aspect of the invention, in an integrated circuit chip including a plurality of metal layers and first and second supply potentials, a programmable memory cell for storing a value is provided, the memory cell comprising:

a first metal interconnect structure that traverses the plurality of metal layers using a first plurality of vias;

a second metal interconnect structure that traverses the plurality of metal layers using a second plurality of vias, wherein prior to programming, said first and second metal interconnect structures are

coupled at a top metal layer; and

an output coupled to one of the first and second supply potentials by at least one of said first and second metal interconnect structures, wherein a state of said output is programmable by altering at least one of the plurality of metal layers.

[0026] Advantageously, the memory cell further comprises multiples of said first and second metal interconnect structures coupled together to form a plurality of programmable cycles for the memory cell, wherein each half cycle is programmable at least once.

[0027] Advantageously, one cycle is laid out to form a ladder structure that traverses the plurality of metal layers from a bottom metal layer to a top metal layer and back to the bottom metal layer.

[0028] Advantageously, said ladder structure is arranged to form a cube-shaped structure.

[0029] Advantageously, the first and second supply potentials comprise two buses located in a central region of said cube-shaped structure and are accessible at each of the metal layers.

[0030] Advantageously, said ladder structure is arranged to form a spiral-shaped structure.

[0031] Advantageously, the first and second supply potentials comprise buses accessible at each of the metal layers.

[0032] Advantageously, each of said first and second metal interconnect structures can be reprogrammed repeatedly by altering any one of the plurality of metal layers.

[0033] Advantageously, each of said first and second metal interconnect structures can be reprogrammed repeatedly by altering any one of a plurality of via layers.

[0034] According to an aspect of the invention, in an integrated circuit chip including a plurality of metal layers and first and second supply potentials, a programmable memory cell for storing a value is provided, the memory cell comprising:

a first metal interconnect structure that traverses the plurality of metal layers using a first plurality of vias;

a second metal interconnect structure that traverses the plurality of metal layers using a second plurality of vias,

an output coupled to one of the first and second supply potentials by at least one of said first and second metal interconnect structures, wherein each of said first and second metal interconnect structures can be programmed repeatedly by altering any one of the plurality of metal layers and any one of a plurality of via layers.

[0035] Advantageously, said first and second metal interconnect structures are not electrically coupled to each other at a top metal layer thereby forming two outputs for the memory cell.

[0036] Advantageously, one of said first and second metal interconnect structures is coupled to the first supply potential at a bottom metal layer and the other of said first and second metal interconnect structures is coupled to the second supply potential at the bottom metal layer.

[0037] Advantageously, said first and second metal interconnect structures are arranged to form a ladder structure.

[0038] Advantageously, said first and second metal interconnect structures are arranged to form an offset ladder structure.

[0039] Advantageously, said first and second metal interconnect structures are arranged to form a stacked structure.

[0040] Advantageously, said stacked structure comprises first and second alternating metal interconnect patterns.

[0041] Advantageously,

said first alternating metal interconnect pattern comprises first and second interspersed metal traces, and

said second alternating metal interconnect pattern comprises third and fourth interspersed metal traces, and

wherein said third and fourth interspersed metal traces form a mirror image of first and second interspersed metal traces.

[0042] Advantageously, said first plurality of vias interconnect ones of said first and third interspersed metal traces and said second plurality of vias interconnect ones of said second and fourth interspersed metal traces.

[0043] Advantageously, the memory cell is programmed at any metal layer by forming an open circuit in each of said first and second interspersed metal traces of that layer thereby splitting each metal trace into two portions, and coupling together a first portion of said first interspersed metal trace to a first portion of said second interspersed metal trace and coupling together a second portion of said first interspersed metal trace to a second portion of said second interspersed metal trace.

[0044] Advantageously, said open circuits and coupling is not performed in regions where vias are located.

[0045] Advantageously, said programming is reversible during a subsequent chip revision.

[0046] Advantageously, the memory cell is programmed at any of a plurality of via layers by removing two vias and inserting two vias.

[0047] Advantageously, said programming is reversible during a subsequent chip revision.

[0048] Advantageously, one of said first and second metal interconnect structures is coupled to the first supply potential at a bottom metal layer and the other of said first and second metal interconnect structures is coupled to the second supply potential at the bottom metal layer.

[0049] According to an aspect of the invention, in an integrated circuit chip including first and second supply potentials, a method of making a programmable memory cell for storing a value is provided, the method comprising:

forming a plurality of metal layers separated by a plurality of via layers;
forming a first metal interconnect structure that traverses the plurality of metal layers using a first plurality of vias in the plurality of via layers;
forming a second metal interconnect structure that traverses the plurality of metal layers using a second plurality of vias in the plurality of via layers;
coupling together said first and second metal interconnect structures at a top metal layer prior to programming;
coupling one of the first and second supply potentials to at least one of said first and second metal interconnect structures to form an output; and
altering at least one of the plurality of metal layers to thereby program the output.

[0050] Advantageously, the method further comprises forming multiples of the first and second metal interconnect structures and coupling together the first and second metal interconnect structures to form a plurality of programmable cycles for the memory cell, wherein each half cycle is programmable at least once.

[0051] Advantageously, the method further comprises forming a one cycle ladder structure that traverses the plurality of metal layers from a bottom metal layer to a top metal layer and back to the bottom metal layer.

[0052] Advantageously, the method further comprises forming the ladder structure in a shape of a cube.

[0053] Advantageously, the method further comprises forming the first and second supply potentials as two buses located in a central region of said cube-shaped structure and so as to be accessible at each of the metal layers.

[0054] Advantageously, the method further comprises forming the ladder structure in a shape of a spiral.

[0055] Advantageously, the method further comprises forming the first and second supply potentials as buses accessible at each of the metal layers.

[0056] Advantageously, the method further comprises altering any one of the plurality of metal layers to thereby reprogram at least one of the first and second metal interconnect structures.

[0057] Advantageously, the method further comprises repeating the reprogramming.

[0058] Advantageously, the method further comprises altering any one of a plurality of via layers to thereby reprogram at least one of first and second metal interconnect structures.

[0059] Advantageously, the method further comprises repeating the reprogramming.

[0060] Advantageously, the method further comprises altering any one of the plurality of metal layers or any one of a plurality of via layers to thereby reprogram the first and second metal interconnect structures.

[0061] Advantageously, the method further comprises repeating the reprogramming.

[0062] According to an aspect of the invention, in an integrated circuit chip including first and second supply potentials, a method of making a programmable memory cell for storing a value is provided, the method comprising:

forming a plurality of metal layers separated by a plurality of via layers;
forming a first metal interconnect structure that traverses the plurality of metal layers using a first plurality of vias in the plurality of via layers;
forming a second metal interconnect structure that traverses the plurality of metal layers using a second plurality of vias in the plurality of via layers;
coupling together said first and second metal interconnect structures at a top metal layer prior to programming;
coupling the first supply potential to the first interconnect structure and the and second supply potential to the second interconnect structure to form two outputs; and
altering at least one of the plurality of metal layers to thereby program at least one of the outputs.

[0063] Advantageously, the method further comprises coupling one of the first and second metal interconnect structures to the first supply potential at a bottom metal layer and coupling the other of the first and second metal interconnect structures to the second supply potential at the bottom metal layer.

[0064] Advantageously, the method further comprises arranged the first and second metal interconnect structures to from a ladder structure.

[0065] Advantageously, the method further comprises arranged the first and second metal interconnect structures to from an offset ladder structure.

[0066] Advantageously, the method further comprises arranged the first and second metal interconnect structures to from a stacked structure.

[0067] Advantageously, the method further comprises forming the stacked structure using first and second alternating metal interconnect patterns.

[0068] Advantageously, the method further comprises:

forming the first alternating metal interconnect pattern using first and second interspersed metal traces, and
forming the second alternating metal interconnect pattern using third and fourth interspersed metal traces, and
forming the third and fourth interspersed metal traces as a mirror image of first and second inter-

spersed metal traces.

[0069] Advantageously, the method further comprises interconnecting the first and third interspersed metal traces using the first plurality of vias and interconnecting ones of the second and fourth interspersed metal traces using the second plurality of vias.

[0070] Advantageously, the memory cell is programmed at any metal layer by:

forming an open circuit in each of said first and second interspersed metal traces of that layer thereby splitting each metal trace into two portions;
coupling together a first portion of said first interspersed metal trace to a first portion of said second interspersed metal trace; and
coupling together a second portion of said first interspersed metal trace to a second portion of said second interspersed metal trace.

[0071] Advantageously, said open circuits and coupling is not performed in regions where vias are located.

[0072] Advantageously, said programming is reversible during a subsequent chip revision.

[0073] Advantageously, the method further comprises removing two vias and inserting two vias at any of a plurality of via layers to thereby program the memory cell.

[0074] Advantageously, said programming is reversible during a subsequent chip revision.

[0075] Advantageously, the method further comprises coupling one of the first and second metal interconnect structures to the first supply potential at a bottom metal layer and coupling the other of the first and second metal interconnect structures to the second supply potential at the bottom metal layer.

[0076] According to an aspect of the invention, in an integrated circuit chip including a plurality of metal layers and first and second supply potentials, a memory cell circuit for modification of a default register value is provided, the circuit comprising:

a memory cell having
a first metal interconnect structure that traverses the plurality of metal layers using a first plurality of vias, wherein said first metal interconnect structure is coupled to one of said first and second supply potentials,
a second metal interconnect structure that traverses the plurality of metal layers using a second plurality of vias, wherein said second metal interconnect structure is coupled to the other one of said first and second supply potentials, and
an output, wherein a state of said output is programmable by altering any one of the plurality of metal layers or any one of a plurality of via layers;
a register having a data input, a data output and control inputs; and
a control circuit coupled to said control inputs of said register, wherein said control circuit receives a chip reset signal and said memory cell output to thereby force said data output of said register to a default register value that equals said output of said memory cell, regardless of said data input of said register.

[0077] Advantageously, said control circuit comprises logic gates.

[0078] Advantageously, said logic gates include a first and a second NAND gate and an inverter.

[0079] Advantageously, said chip reset signal is input to said first and second NAND gates, said memory cell output is input to said second NAND gate and said inverter, an output of said inverter is input to said first NAND gate, and outputs of said first and second NAND gates are provided to said control inputs of said register.

[0080] Advantageously, said register comprises a flip-flop.

[0081] Advantageously, said flip-flop comprises a D-Q flip-flop.

[0082] Advantageously, prior to programming, said first and second metal interconnect structures are coupled at a top metal layer.

[0083] Advantageously, the circuit further comprises multiples of said first and second metal interconnect structures coupled together to form a plurality of programmable cycles for the memory cell, wherein each half cycle is programmable at least once.

[0084] Advantageously, one cycle is laid out to form a ladder structure that traverses the plurality of metal layers from a bottom metal layer to a top metal layer and back to the bottom metal layer.

[0085] Advantageously, said ladder structure is arranged to form a cube-shaped structure.

[0086] Advantageously, the first and second supply potentials comprise two buses located in a central region of said cube-shaped structure and are accessible at each of the metal layers.

[0087] Advantageously, said ladder structure is arranged to form a spiral-shaped structure.

[0088] Advantageously, the first and second supply potentials comprise buses accessible at each of the metal layers.

[0089] Advantageously, each of said first and second metal interconnect structures can be reprogrammed repeatedly by altering any one of the plurality of metal layers.

[0090] Advantageously, each of said first and second metal interconnect structures can be reprogrammed repeatedly by altering any one of a plurality of via layers.

[0091] Advantageously, each of said first and second metal interconnect structures can be reprogrammed repeatedly by altering any one of the plurality of metal layers and any one of a plurality of via layers.

[0092] Advantageously, said first and second metal interconnect structures are not electrically coupled to

each other at a top metal layer thereby forming two outputs for the memory cell.

[0093] Advantageously, one of said first and second metal interconnect structures is coupled to the first supply potential at a bottom metal layer and the other of said first and second metal interconnect structures is coupled to the second supply potential at the bottom metal layer.

[0094] Advantageously, said first and second metal interconnect structures are arranged to from a ladder structure.

[0095] Advantageously, said first and second metal interconnect structures are arranged to from an offset ladder structure.

[0096] Advantageously, said first and second metal interconnect structures are arranged to from a stacked structure.

[0097] Advantageously, said stacked structure comprises first and second alternating metal interconnect patterns.

[0098] Advantageously,

said first alternating metal interconnect pattern comprises first and second interspersed metal traces, and

said second alternating metal interconnect pattern comprises third and fourth interspersed metal traces, and

wherein said third and fourth interspersed metal traces form a mirror image of first and second interspersed metal traces.

[0099] Advantageously, said first plurality of vias interconnect ones of said first and third interspersed metal traces and said second plurality of vias interconnect ones of said second and fourth interspersed metal traces.

[0100] Advantageously, the memory cell is programmed at any metal layer by forming an open circuit in each of said first and second interspersed metal traces of that layer thereby splitting each metal trace into two portions, and coupling together a first portion of said first interspersed metal trace to a first portion of said second interspersed metal trace and coupling together a second portion of said first interspersed metal trace to a second portion of said second interspersed metal trace.

[0101] Advantageously, said open circuits and coupling is not performed in regions where vias are located.

[0102] Advantageously, said programming is reversible during a subsequent chip revision.

[0103] Advantageously, the memory cell is programmed at any of a plurality of via layers by removing two vias and inserting two vias.

[0104] Advantageously, said programming is reversible during a subsequent chip revision.

[0105] Advantageously, one of said first and second metal interconnect structures is coupled to the first supply potential at a bottom metal layer and the other of said first and second metal interconnect structures is coupled to the second supply potential at the bottom metal layer.

[0106] In an integrated circuit chip including a plurality of metal layers, first and second supply potentials and at least two adjacent logic blocks, a modifiable circuit for coupling the at least two adjacent logic blocks is provided, comprising:

a first metal interconnect structure that traverses the plurality of metal layers using a first plurality of vias, wherein said first metal interconnect structure is located at a boundary of the at least two adjacent logic blocks;

a second metal interconnect structure that traverses the plurality of metal layers using a second plurality of vias, wherein said second metal interconnect structure is located at said boundary of the at least two adjacent logic blocks; and

an interconnect formed between the at least two adjacent logic blocks by at least one of said first and second metal interconnect structures, wherein a state of said interconnect is programmable by altering any one of the plurality of metal layers or any one of a plurality of via layers.

[0107] Advantageously, said first metal interconnect structure is coupled to one of said first and second supply potentials and said second metal interconnect structure is coupled to the other one of said first and second supply potentials.

[0108] Advantageously, prior to programming, said first and second metal interconnect structures are coupled at a top metal layer.

[0109] Advantageously, the circuit further comprises multiples of said first and second metal interconnect structures coupled together to form a plurality of modifiable cycles, wherein each half cycle is modifiable at least once.

[0110] Advantageously, one cycle is laid out to form a ladder structure that traverses the plurality of metal layers from a bottom metal layer to a top metal layer and back to the bottom metal layer.

[0111] Advantageously, said ladder structure is arranged to form a cube-shaped structure.

[0112] Advantageously, the first and second supply potentials comprise two buses located in a central region of said cube-shaped structure and are accessible at each of the metal layers.

[0113] Advantageously, said ladder structure is arranged to form a spiral-shaped structure.

[0114] Advantageously, the first and second supply potentials comprise buses accessible at each of the metal layers.

[0115] Advantageously, each of said first and second metal interconnect structures can be reprogrammed repeatedly by altering any one of the plurality of metal layers.

[0116] Advantageously, each of said first and second

metal interconnect structures can be reprogrammed repeatedly by altering any one of a plurality of via layers.

[0117] Advantageously, each of said first and second metal interconnect structures can be reprogrammed repeatedly by altering any one of the plurality of metal layers and any one of a plurality of via layers.

[0118] Advantageously, said first and second metal interconnect structures are not electrically coupled to each other at a top metal layer thereby forming two interconnects between the at least two adjacent logic blocks.

[0119] Advantageously, one of said first and second metal interconnect structures is coupled to the first supply potential at a bottom metal layer and the other of said first and second metal interconnect structures is coupled to the second supply potential at the bottom metal layer.

[0120] Advantageously, said first and second metal interconnect structures are arranged to form a ladder structure.

[0121] Advantageously, said first and second metal interconnect structures are arranged to form an offset ladder structure.

[0122] Advantageously, said first and second metal interconnect structures are arranged to form a stacked structure.

[0123] Advantageously, said stacked structure comprises first and second alternating metal interconnect patterns.

[0124] Advantageously:

said first alternating metal interconnect pattern comprises first and second interspersed metal traces, and

said second alternating metal interconnect pattern comprises third and fourth interspersed metal traces, and

wherein said third and fourth interspersed metal traces form a mirror image of first and second interspersed metal traces.

[0125] Advantageously, said first plurality of vias interconnect ones of said first and third interspersed metal traces and said second plurality of vias interconnect ones of said second and fourth interspersed metal traces.

[0126] Advantageously, the memory cell is programmed at any metal layer by forming an open circuit in each of said first and second interspersed metal traces of that layer thereby splitting each metal trace into two portions, and coupling together a first portion of said first interspersed metal trace to a first portion of said second interspersed metal trace and coupling together a second portion of said first interspersed metal trace to a second portion of said second interspersed metal trace.

[0127] Advantageously, said open circuits and coupling is not performed in regions where vias are located.

[0128] Advantageously, said programming is reversible during a subsequent chip revision.

[0129] Advantageously, the memory cell is programmed at any of a plurality of via layers by removing two vias and inserting two vias.

[0130] Advantageously, said programming is reversible during a subsequent chip revision.

[0131] Advantageously, one of said first and second metal interconnect structures is coupled to the first supply potential at a bottom metal layer and the other of said first and second metal interconnect structures is coupled to the second supply potential at the bottom metal layer.

[0132] Further embodiments, features, and advantages of the present inventions, as well as the structure and operation of the various embodiments of the present invention, are described in detail below with reference to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS/FIGURES

[0133] The accompanying drawings, which are incorporated herein and form a part of the specification, illustrate the present invention and, together with the description, further serve to explain the principles of the invention and to enable a person skilled in the pertinent art to make and use the invention.

[0134] FIG. 1 illustrates a schematic block diagram of revision identification (ID) bits.

[0135] FIG. 2 illustrates a meta-memory cell (MMCEL) according to an embodiment of the present invention.

[0136] FIGs. 3A-3C illustrate an MMCEL according to the present invention.

[0137] FIG. 4 illustrates another MMCEL embodiment according to the present invention.

[0138] FIGs. 5A and 5B illustrate a 3-D spiral layout for an MMCEL 500 according to the present invention.

[0139] FIG. 6 illustrates a dual output MMCEL, according to the present invention.

[0140] FIG. 7A illustrates a basic layout structure for an enhanced dual output MMCEL according to the present invention.

[0141] FIG. 7B illustrates MMCEL 700 with initial programming according to the present invention.

[0142] FIG. 7C illustrates a RevID<0> layout change according to the present invention.

[0143] FIG. 7D illustrates a further revision of the MMCEL 700 according to the present invention.

[0144] FIG. 8A shows vertically stacked MMCEL layout patterns according to the present invention.

[0145] FIG. 8B shows staircase MMCEL layout patterns according to the present invention.

[0146] FIGs. 9A, 9B, 9C and 9D illustrate the basic MMCEL switching of the dual output MMCEL according to the present invention.

[0147] FIGs. 10A and 10B illustrate a basic MMCEL metal and via layer pattern template according the

present invention.

[0148] FIGs. 11A-D illustrate MMCEL layout edit rules for metal changes according to the present invention.

[0149] FIGs. 12A-12D describe MMCEL via edit rules according to the present invention.

[0150] FIG. 13 illustrates MMCEL basic pattern layout permutations according to the present invention.

[0151] FIG. 14 illustrates an MMCEL flip basic pattern layout permutation according to the present invention.

[0152] FIGs. 15A-15D illustrate a triple metal MMCEL stack layout example according to the present invention.

[0153] FIGs. 16, 17A-C, 18A-C, 19A-C, 20A-C and 21A-C illustrate an MMCEL layout in a six metal layer implementation according to the present invention.

[0154] FIG. 22 illustrates the use of FIB technology for programming the MMCEL of the present invention.

[0155] FIG. 23 illustrates a register having a modifiable default value according to the present invention.

[0156] FIG. 24 illustrates an MMCEL architecture used in a ROM (Read-Only-Memory) array according to the present invention.

[0157] FIG. 25 illustrates meta-connect cells (MCCEL) according to the present invention.

[0158] FIGs. 26A, 26B, 27, 28A-28D, 29A, 29B, 30, 31, 32A-32D, 33A-33D, 34A, 34B, 35A, 35B, 36A, 36B, 37, 38A, 38B, 39A and 39B illustrate circuits employing MCCEL and/or MMCELs according to the present invention.

[0159] The present invention will now be described with reference to the accompanying drawings. In the drawings, like reference numbers indicate identical or functionally similar elements. Additionally, the left-most digit(s) of a reference number identifies the drawing in which the reference number first appears.

DETAILED DESCRIPTION OF THE INVENTION

[0160] The preferred embodiment of the present invention will now be discussed in detail. While specific features, configurations and arrangements are discussed, it should be understood that this is done for illustration purposes only. A person skilled in the relevant art will recognize that other steps, configurations and arrangements or devices may be used to achieve the features of the invention without departing from the spirit and scope thereof. Indeed, for the sake of brevity, conventional electronics, manufacturing of semiconductor devices, and other functional aspects of the method/apparatus (and components of the individual operating components of the apparatus) may not be described in detail herein.

[0161] The terms chip, integrated circuit, monolithic device, semiconductor device, and microelectronic device are often used interchangeably in this field. The present invention is applicable to all the above as they are generally understood in the field.

[0162] The material commonly used to form conductors in semiconductor integrated circuit chips is metal, such as copper, aluminum, various alloys, polycrystalline silicon (polysilicon), and the like. The term "metal" will be used herein to cover any type of conductor, including but not limited to the foregoing metals and polysilicon. The terms conductive line or path, strips and traces are used interchangeably herein to refer to a metal conductor. Metal layers will be referred to by number, such as M3 for metal layer three, and so on.

[0163] The term "via" as used herein refers to an area or opening in a dielectric layer that provides an electrical pathway from one metal layer to the metal layer above or below. The electrical pathway comprises a metal that fills the via. Alternatively, the via walls are made conductive.

[0164] Further, background material concerning semiconductor solid-state physics and manufacturing can be found in a number of publicly available references including two books by S.M. Sze, titled: Physics of Semiconductor Devices, John Wiley and Sons, Inc., New York (1981), and Semiconductor Devices, Physics and Technology, John Wiley and Sons, Inc., New York (1985), both of which are incorporated herein by reference.

[0165] It should be understood that the spatial descriptions (e.g., "above", "below", "up", "down", etc.) made herein are for purposes of illustration only.

[0166] The invention is directed to a circuit, called a Meta-Memory Cell (MMCEL), to facilitate the modifications of the revision ID bits at any metal or via layer. The required number of metal layers for the next design iteration is greatly reduced by the MMCEL because the revision ID bit changes can be made on the same metal layer as the logic design fix.

[0167] The MMCEL resembles a hard-wired memory cell with dual complementary outputs. The MMCEL utilizes all layers of metal including metal vias to fully meet its design requirement. Unlike a silicon-based nonvolatile programmable memory, the MMCEL does not require active silicon (i.e., the base layers) to retain a programmed logic value. Instead, it relies only on the alteration of any single metal or via layer for re-programming. When inserted into existing chip designs, only one metal or via layer change is required to utilize the MMCEL.

[0168] The following figures and accompanying description more fully describe the present invention.

[0169] FIG. 1 illustrates a schematic block diagram of revision identification (ID) bits. A plurality of revision ID bits RevID <0> through RevID <x> are combined to form a revision identification word RevID<x : 0>. The revision identification word typically comprises 8 bits, but may comprise 16 bits, 32 bits, or the like, as would be apparent to a person having ordinary skill in the art.

[0170] FIG. 2 illustrates a single meta-memory cell (MMCEL) according to an embodiment of the present invention. According to this embodiment, MMCEL 200 comprises cycles 1 through Y. Each MMCEL cycle comprises two ladders (e.g., 202 and 204) that traverse layers of an integrated circuit (five metal layers are depict-

ed, for example). Each horizontal rung of the serpentine ladder structure is formed of metal traces at any one of metal layers 1-5 (M1-M5). Each vertical rung of the ladder structures comprises a via formed in a material layer between any two adjacent metal layers, as would also be apparent to a person having ordinary skill in the art.

[0171] A plurality of MMCELs (each comprising a given number of cycles) form a single revision identification word. For example, an 8 bit revision identification word would comprise eight MMCELs.

[0172] The number of whole cycles that an MMCEL has depends on the number of revisions a integrated circuit designer contemplates for a given integrated circuit during the production life of that integrated circuit.

[0173] FIG. 3A illustrates an MMCEL having the beginning of cycle one tied to ground (logic 0) at M1. The output of this MMCEL 300 is provided at the end of cycle Y, also at M1, and provides revision ID output RevID <0>. Thus, the output of MMCEL 300 is a logic 0.

[0174] FIG. 3B illustrates a modification to MMCEL 300. In order to change the value of MMCEL 300 output RevID <0> during a later revision of the integrated circuit, the interconnected metal ladders of cycles one through cycle Y must be changed. In this example, the first revision to the integrated circuit is performed in cycle one of MMCEL 300. Assuming that a revision to the integrated circuit is made to the mask corresponding to M5, this layer will be used to modify the revision bit. This avoids having to make modifications to any other mask in the manufacturing process. In this case, the metal trace at cycle one on M5 is tied to a power supply (e.g., VDD or logic 1). Tying the ladder 204 of cycle one to VDD inverts the output of MMCEL 300 from logic 0 to logic 1.

[0175] Providing each cycle of the MMCEL with two ladders permits at a minimum of two revisions per cycle of the MMCEL. For example, an MMCEL comprising three full cycles can be modified a minimum of 6 times in order to implement numerous modifications to the revision bit. More revisions per cycle are possible, depending on which metal layers are modified and in what order per chip revision.

[0176] FIG. 3C illustrates another revision to cycle one in which ladder 204 is tied to ground (logic 0) on M3. This change causes the RevID <0> value to invert from logic 1 (as shown in FIG. 3B) back to logic 0.

[0177] Another MMCEL embodiment is illustrated in FIG. 4. Rather than the serpentine ladder illustrated in FIGs. 2 and 3A-C, the MMCEL of FIG. 4 is laid out in the shape of a 3-dimensional (3-D) cube. MMCEL 400 comprises two cycles. Power (VDD) and ground (GND) buses are formed in the center of the 3-D cube layout. This permits access to power and ground by any of the four half cycles at any of the metal layers M1-M5. Alternatively, power and ground buses can be placed external to the main structure. The internal metal widths of the traces should be wide enough to accommodate a low resistant path between this MMCEL and any adjacent circuit. Due to long trace routs when using this MMCEL structure, designers should be aware of the resistance-capacitance (RC) delay and its consequences within the integrated circuit. Buffers can be added within the structure as necessary to improve signal transmission along long routing paths, as would be apparent to a person having ordinary skill in the art.

[0178] FIGS. 5A and 5B illustrate a 3-D spiral layout for an MMCEL 500. The spiral approach allows stacking of cycles to create greater than two cycles per cell as compared to MMCEL 400 of FIG. 4, for example. The power and ground buses are made available along the outside of the cell. Only two power and ground buses are illustrated at metal layer one in FIGS. 5A and 5B to simplify the drawing. However, power and ground buses should be provided at all metal layers for optimum programmability of the revision bit. An inter-cell connect trace is illustrated at 502, which couples cycle number one and cycle number two.

[0179] The present invention simplifies the layout by eliminating the tedious work of routing the revision identification on the same layer as the design modifications to the integrated circuit. The layout changes are made locally at a predefined location according to the present invention. Moreover, no ERC or DRC violations occur according to the present invention because layout changes do not leave a floating metal trace; disconnected metal traces are tied to either ground or power.

[0180] A dual output MMCEL is illustrated in FIG. 6, according to another embodiment of the present invention. The dual output cell outputs a logic 1 and a logic 0 at outputs 602, 604, respectively. This MMCEL resembles a hard-wired memory cell with dual complementary outputs that is implemented on metal layers only. The MMCEL utilizes all layers of metal including metal vias to fully meet its design requirement.

[0181] A basic layout structure for an enhanced dual output MMCEL is illustrated in FIG. 7A. Dual output MMCEL 700 comprises 2 metal ladders 702 and 704, which traverse all metal layers of the integrated circuit, such as metal layers M1-M6, for example.

[0182] The dual parallel metal ladder structure can traverse each metal and via layer of the chip. This allows the output of the MMCEL to be inverted at any metal or via layer. In addition, the dual parallel metal ladder structure enables the MMCEL unlimited design iterations. Thus, the output of the MMCEL can be inverted as often as required.

[0183] In accordance with the dual parallel metal ladder structure of the MMCEL, one metal ladder is connected to power (VDD) at the bottom layer M1 and another metal ladder is connected to ground (GND) also at M1. Both metal ladders reach the top metal layers (for example, M5 layer for 0.18μm technology, M6 layer for 0.13μm technology) depending on the requirements of the user. The outputs of the MMCEL come from a top layer connection to the metal ladders, as described below.

[0184] FIG. 7B illustrates MMCEL 700 with initial programming such that ladder 702 is coupled to power (VDD) at M1 and ladder 702 is coupled to ground (GND) at M1. Coupling ladder 702 to power and ladder 704 to ground produces a logic 1 and a logic 0 output, respectively. The MMCEL output RevID<0> can be selected at either output.

[0185] According to the present invention, the dual output MMCEL accommodates both single layer metal or single layer via changes in order to modify the output of the MMCEL. An infinite number of changes on any single layer of metal or single layer via can be performed at each cell.

[0186] FIG. 7C illustrates a RevID<0> layout change from logic 0 to logic 1 on M5 only. As shown at region 706, the metal traces of ladders 702 and 704 are cross-connected in order to invert both outputs of the dual MMCEL 700. This cross connection is achieved by altering the metal layer by forming two cuts and two jumps. Alternatively, the cross connection can be achieved by simultaneously moving two vias to form an alternative interconnection, as will be described below.

[0187] Turning to FIG. 7D, a further revision of the MMCEL 700 can be performed at another metal layer, such as M3. Again, the metal traces of ladder 702 and 704 are cross-connected at M3, as shown generally at a region 708. This second revision of the output of MMCEL 700 returns the output of ladder 702 to a logic 1 state and the output of ladder 704 to a logic 0 state. Of course, if subsequent revisions of the integrated circuit are performed on the same metal layer the two cuts and jumps as described in connection with cross connection 706, for example, could simply be reversed in order to change the output of the MMCEL.

[0188] The dual output MMCEL of the present invention can be implemented using stacked layers of the same layout pattern. Two such stacking approaches are shown in FIGs. 8A and 8B. FIG. 8A shows a vertically stacked layer approach. The stacked structure of FIG. 8A comprises alternating layers labeled type A and type B. Type A is hereafter referred to as a normal pattern and type B as a flipped pattern. The flipped pattern B is a mirror image of the normal pattern A, as will be described below.

[0189] FIG. 8B shows a staircase of layers all having the same type A layout pattern. The staircase layer approach requires more chip real estate to implement than the stacked layer approach of FIG. 8A. Both of the stacked and staircase layer approaches are achieved by aligning the output vias of the bottom layer to the input vias of the top layer, as described below.

[0190] First, however, the basic switching of the dual output MMCEL will be described in connection with schematic diagrams of FIGs. 9A and 9B. An exemplary metal or via layer having two inputs (labeled A_in and B_in) and two outputs (labeled A_out and B_out). The schematic diagram of FIG. 9B shows electrically equivalent double pull double throw (DPDT) switches for each metal change or via change. DPDT switch SW1 represents a metal change and DPDT switch SW2 represents a via change. The logic convention assigned to the switches is that a switch in the 'up' position equates to a logic '0' and in the 'down' position equates to a logic '1'. The following logic table (Table 1) demonstrates how the output can be modified according to the state of switches SW2 and SW1:

Table 1

SW2	SW1	A_out	B_out
0	0	a_in	b_in
0	1	b_in	a_in
1	0	b_in	a_in
1	1	a_in	b_in

[0191] FIGs. 9C and 9D illustrate metal vias inserted between the "b" and "t" via locations to connect the bottom layer metal wires to the top layer metal wires. Via location "b" means bottom input and via location "t" means top output. FIG. 9C shows a connection between the bottom layer metal wire 1 and the top layer metal wire 1. Also, there is a connection between the bottom layer metal wire 2 and the top layer metal wire 2. FIG. 9D shows the result of two metal via disconnection and two metal via connection starting from FIG. 9C. As a result, FIG. 9D shows a connection between the bottom layer metal wire 1 and the top layer metal wire 2. Also, there is a connection between the bottom layer metal wire 2 and the top layer metal wire 1. Hence, the configuration of FIG. 9D effectively emulates the effect of a double-pull double-throw switch that cross connects the metal wires between the bottom and top metal layers, as described above in connection with FIG. 9B.

[0192] FIGs. 10A and 10B illustrate a basic metal and via layer pattern template according to the present invention. Input vias that connect to a bottom metal layer are labeled "b", while output vias that connect to the top metal layer are labeled "t". Metal traces of the pattern template are shown as solid black lines. The position of bottom vias on a current layer is determined by the position of corresponding top vias on an adjacent bottom metal layer. Therefore, for single via layer changes, only output vias on the current layer are allowed to be moved and input vias remain fixed. This is illustrated in FIG. 10B.

[0193] Space is allocated to make the metal edits (cuts and jumps) and also to remove and place the vias. Layout rules are used, such as "keep-out" sections where the metal edits can be implemented along with specific via placement locations. These layout rules ensure the functional integrity of the MMCEL for future modifications. Two keep-out sections surrounding the input vias and output vias are shown in FIG. 10B.

[0194] The two bottom (input) vias on the left keep-

out area of FIG. 10B are labeled 1 and 2, respectively. Similarly, the two top (output) vias are also labeled 1 and 2 respectively, on the right keep-out area of FIG. 10B. The darker shaded numbers 1 and 2 on both the left and right portion of FIG. 10B correspond to the initial locations of the input and output vias of FIG. 10A. A via change comprises relocating the via layer pattern from the initial positions to new positions illustrated by the dashed boxes and arrows at FIG. 10B. MMCEL layout edit rules for via changes will be described in more detail below.

[0195] In an embodiment of the present invention, the logic state of the MMCEL outputs can be inverted simultaneously by following the MMCEL's own layout design edit rules in altering a metal or via layer. There are basically four metal layer edit rules and four metal via edit rules. These rules ensure that current layout changes inside the MMCEL preserve the functionality and integrity of the MMCEL. Also, the edit rules are designed to allow future changes to the metal structure of the same MMCEL, since revision ID bits or default register values often change more than once. Hence, the MMCEL has the unlimited capability to be modified by a user in order to invert its output values at any single metal or via layer.

[0196] FIGs. 11A-D illustrate MMCEL layout edit rules for metal changes. A basic metal and via layer pattern template is illustrated in FIG. 11A and a flip basic pattern is illustrated in FIG. 11C. The basic pattern of FIG. 11A is used in the odd metal layers (e.g., M1, M3, M5, etc.). The flip basic pattern is used in even metal layers (e.g., M2, M4, M6, etc.). Reversal of these patterns (i.e., basic on even metal layers and flip on odd) is also contemplated.

[0197] The MMCEL metal edit rule comprises two cuts and two jumps in order to implement a metal change for either the basic pattern or the flip basic pattern. FIG. 11B shows two cuts 1102 and 1104 and two jumps 1106 and 1108 used to implement a basic pattern metal change. Similarly, FIG. 11D shows two cuts 1110 and 1112, as well as two jumps 1114, 1116, which implement the flip basic pattern metal change.

[0198] MMCEL via edit rules will now be described in connection with FIGs. 12A-12D. FIGs. 12A and 12B illustrate the basic metal and via layer pattern template. FIGs. 12C and 12D show the flip basic pattern. In order to implement a via edit on the basic pattern, two disconnects and connects of vias are required. A first via (labeled "1") is disconnected from trace 1202 and a connection is made to trace 1204. Additionally, a second via (labeled "2") is disconnected from metal trace 1204 and then connected to trace 1202, as shown in FIG. 12B. The order in which the disconnects and connects are performed is irrelevant. Similarly, a via edit for the flip basic pattern is shown in FIG. 12D. Via 1 is disconnected from trace 1204 and then connected to trace 1206, while via 2 is disconnected from trace 1206 and then connected to trace 1204.

[0199] FIG. 13 illustrates MMCEL basic pattern layout permutations. Four patterns are shown, including pattern A, pattern B, pattern C and pattern D. Beginning with pattern A, a via change according to the above described rules results in what is shown in pattern B. Alternatively, starting at pattern A, a metal change according to the above-described rules results in what is shown at pattern D. Thus, the via disconnects and connects and metal cuts and jumps are illustrated for each metal or via permutation starting with any one of the four patterns. Similarly, FIG. 14 illustrates an MMCEL flip basic pattern layout permutation. Four patterns are shown including pattern E, pattern F, pattern G and pattern H. Again, all via disconnects and connects and metal cuts and jumps required to move from one pattern to another pattern are shown in FIG. 14 for the flip basic pattern.

[0200] The vias labeled 1 and 2 in FIGs. 13 and 14 represent the top vias described above in connection with basic patterns. Thus, the vias labeled "b" in FIGs. 13 and 14 are provided at these locations by way of example and not limitation. In other words, in an actual implementation the positioning of the b vias will depend upon the positioning of the vias coupled to a lower metal layer. Therefore, the b vias shown on FIGs. 15A-15D do not correspond specifically to the b vias of FIGs. 13 and 14, because their position is dependent upon the location of each underlying metal layer via, as addressed above in connection with FIGs. 10A & 10B.

[0201] FIGs. 15A-15D illustrate a triple metal stack layout example according to the present invention. Basic pattern layouts are shown at the bottom and top of each one of FIGs. 15A-15D that are associated with M1 and M3, respectively. A flip basic pattern is shown in the middle of the stack in each of FIGS. 15A-15D, and corresponds to M2. Each basic or flip pattern layout of FIGS. 15A-15D are also labeled as pattern A through pattern H as described above in connection with FIGS. 13 and 14.

[0202] An initial structure of the stack layout example is shown in FIG. 15A. The basic layout pattern at M1 in FIG. 15A shows a first metal trace tied to ground having a first via labeled "1", and a second metal trace tied to power and coupled to a second via labeled "2". The flip basic pattern E of FIG. 15A has a first metal trace with vias labeled "b" and "2". Via b electrically couples the first metal trace at M2 to the first metal trace of M1 at the same via, as illustrated by vertical lines 1502. Thus, the first metal trace of the flip basic pattern E at M2 is also coupled to ground.

[0203] A second metal trace of flip pattern E at M2 is coupled to two vias labeled "1" and "b". As described above, the vias labeled "b" indicate that via is coupled electrically to a bottom metal layer. Thus, the second trace of flip pattern E is electrically coupled to the second metal trace of basic pattern A at M1, and is thus coupled to power.

[0204] The right most vias at M2 couple the first and second traces of flip basic pattern E to the metal traces at M1. The two left most vias of flip basic pattern E at

M2 couple the M2 traces to the M3 traces stacked thereon. In this arrangement, the via labeled "2" couples the first trace of a flip basic pattern E at M2 to a first metal trace of basic pattern A at M3. This coupling is shown at 1504. The output RevID<0> of this MMCEL is a logic 0 as provided at a top via labeled "1" on the first metal trace of basic pattern A at M3. Although not shown on this figure, a logic 1 is available at the second top via labeled "2" on the second metal trace of basic pattern A at M3.

[0205] FIG. 15B illustrates a metal change at the center layer of the stack layout shown in FIG. 15A. The metal change at center layer represents basic pattern H shown in FIG. 14. Based on this change, which includes two cuts and two jumps, the right most via b at the center layer is now electrically coupled via a metal trace to the second top via at the center layer, which in turn is coupled to the first trace at M3. This metal layer change at the center layer causes the RevID<0> to change from a logic 0 to a logic 1. While the signal coupling to the top via labeled "1" at M3 is provided to M2 as in 1504 in FIG. 15A, the operative coupling between M2 and M1 is now provided by the other bottom via of M2 as shown at 1506.

[0206] **[00100]** FIG. 15C illustrates a via change at the center layer. Because a via change is at the center layer, the flip basic pattern now corresponds to pattern G of FIG. 14. Thus, via 1 of pattern A at M1 provides a ground signal to M2, which in turn provides ground to M3 at via 2 of flip pattern G. These connections are shown at 1508 and 1510, respectively. Accordingly, the output at M3 via 1 is changed from a logic 1 to a logic 0.

[0207] **[00101]** A final revision example is shown in FIG. 15D, which comprises a metal change at the center layer. In this case, via 2 of M1 is used to couple power to M2. Using the flip pattern F, the second via of M2 is used to couple power to M1, as shown at 1512 and 1514, respectively. In this manner via 1 of M3 is switched from logic level 0 to logic level 1.

[0208] **[00102]** FIGs. 16, 17A-C, 18A-C, 19A-C, 20A-C and 21A-C illustrate an MMCEL layout in a six metal layer implementation according to the present invention.

[0209] **[00103]** This exemplary MMCEL layout is implemented in layer M6 0.13μm semiconductor manufacturing technology. Other known and future technologies employing metal (e.g, 0.18μm aluminum, 0.13μm copper, etc.), doped polysilicon, and the like, can be used as would be apparent to a person having ordinary skill in the art.

[0210] **[00104]** FIG. 16 shows all layers of the stacked structure. FIG. 17A shows M1 and via layer 1. FIG. 17B shows M2. FIG. 17C shows an overlay of M1, via 1 and M2 layers. FIGs. 18-21 show the remaining metal and via layers of the stacked structure. The dimensions shown in the figure are presented for illustration, and are intended to being limiting.

[0211] [00105] Layout blocks implemented with conventional "standard cells" have rows of same-height cells that abut as much as possible. Any gaps between the cells are typically filled with "filler" cells. These filler cells contain geometries to extend certain layers across the gaps, such as power straps and well implant. The gaps between the "standard cells" are caused by the ineffiency of the routing tool used by the layout designer. In order to comply with Design Rule Check (DRC) requirements, these gaps must be filled with the same basic material used in the "standard cells" in order to preserve the power supply and base layer connections. The chip will not function correctly if the filler cells are not inserted between the gaps.

[0212] **[00106]** One implementation of the MMCEL or MCCEL is a design that starts with a filler cell that has the same layout structure and size as a "Filler_16" cell so that all base layers will match. The only modifications the inventors needed to make were changes to the metal and via layers. For existing designs, the MMCEL or MCCEL becomes drop-in compatible for all metal layer changes. This enables the designers to instantiate a new MMCEL or MCCEL even after the base layers have been fabricated. The main advantages of using "Filler_16" are availability of existing "standard cells", drop-in capability, and no electrical impact to existing design.

[0213] [00107] Using the "standard cell" approach, an MMCEL layout in accordance with an embodiment of the present invention can meet the requirements for focused ion beam (FIB) anisotropic etching to implement edits. Ample space may be provided between the MMCEL's metal interconnect on the top metal layer so that a cut and a jump can be successfully implemented without creating a short. The FIB area can be located at the highest metal layer where it is readily accessible.

[0214] [00108] FIG. 22 illustrates the use of FIB technology for programming the MMCEL of the present invention. A FIB free space region is shown generally at 2202. Two parallel metal strips (traces) are shown generally at 2204. A cut of a metal trace is illustrated generally at 2206. A jump between two metal traces is shown at 2208. Metal "cuts" require more free space than metal deposition. Distance between parallel metal strips is dictated by design rules.

[0215] [00109] An MMCEL design in accordance with an embodiment of the present invention can also be used not only for revision ID applications, but also for programming the default values of internal registers. These internal registers basically define the operating modes of the chip and altering its default values causes the chip to behave in another desired functionality. If planned well enough in advance, the MMCEL can be used to meet specific requirements from different customers and provide a variety of applications for a single chip design.

[0216] [00110] Conventional methodologies for providing a programmable revision ID bit includes both silicon-based and metal only based designs. The silicon-

based designs are implemented as programmable Non-Volatile Memory (PROM) where the default values are stored in a memory cell. The PROM is read at start-up and the contents used to initialize the revision ID bits or default registers. The advantages of this approach are ease of use and flexibility in implementation. However, there are also several drawbacks when compared to an MMCEL in accordance with an embodiment of the present invention. For example, the PROM requires an all-layer change, whereas the MMCEL only requires edits to one metal or via layer. The PROM requires additional support circuitry such as registers and programming logic, whereas the MMCEL requires none. The PROM-based method is less reliable than the MMCEL because the memory can lose retention unlike the MMCEL, which is hardwired and permanent (at least until a subsequent edit changes the value of the output of the MMCEL). Once implemented, the advantages of the MMCEL over the PROM-based design are that the MMCEL is cheaper, smaller in area, and provides better reliability.

[0217] [00111] FIG. 23 illustrates a circuit 2300 comprising a register 2302, logic 2304, NAND gates 2306 and 2308, and an inverter 2310. The register 2302 is depicted as a DQ flip-flop, but need not be as would apparent to a person having ordinary skill in the art. Register 2302 has a data input (D), a data output (Q), a pair of inputs (clear ('CLR') and 'SET'), and a clock input (CLK). The clock input CLK can be used in connection with a synchronous circuit, but is not necessary and is not employed in this embodiment. Logic 2304 provides a logic high or a logic low input to the register 2302.

[0218] [00112] Upon receipt of a Reset signal, circuit 2300 will permit the value of logic 2300 to propagate to the output of the register 2302 depending on the state of MMCEL output. The Reset signal is applied to inputs of the NAND gates 2306 and 2308. The MMCEL output is applied to the input of NAND gate 2306, which has its output connected to the SET input of register 2302. The MMCEL output is also applied to an input of NAND gate 2308 through the inverter 2310. The output NAND gate 2308 is provided to the clear input (CLR) of register 2302. The value of the MMCEL output coupled with the value of a Reset signal generates a register output (REG_Q) according to the following table:

Table 2

Reset	MMCEL	Reg_Q
0	0	Q
0	1	Q
1	0	0
1	1	1

[0219] [00113] The above functionality can be preformed by other combinational logic, as would become apparent to a person having ordinary skill in the art.

[0220] **[00114]** The meta-memory cells of the present invention can be implemented as a library cell for ease of use among chip projects. 16, 8, 4, 2, 1 and ½ cycle cells can be used, for example. As is described above, each cell type has a preprogrammed output such as logic 1 or logic 0.

[0221] **[00115]** Memory cells of the present invention (e.g., the MMCEL) can be used in a variety of circuits. For example, MMCEL architecture can be used in ROM (Read-Only-Memory) arrays, which is illustrated in FIG. 24. The ROM array includes multiplexers 2402 whose inputs are single memory bits each driven by an MMCEL 2404. Only one of first and second output terminals (Out_1 or Out_2) of the MMCEL 2404 is connected to a top one of the multiplexers 2402 at one time. The Address<M:0> signal is routed to control select lines of multiplexers 2402 to choose from 2^(M+1) address bits. The number of MMCELs 2404 per multiplexer 2402 dictates a width of an address bus. A Data<N:0> terminal is connected to outputs of each of multiplexer 2402 to form an (N+1) width data bus. A number of parallel multiplexers 2402 dictates the width of the data bus. The entire contents of the ROM array can be changed within a single metal layer or a single via layer because the MMCELs 2404 are used as the basic memory cell component. Accordingly, a ROM array implemented in such a manner significantly reduces the cost of modifying the ROM array due to, for example, changes in the customer's software requirements or bugs in the software implementation.

[0222] **[00116]** The meta-memory cells of the present invention can be implemented as a library cell for ease of use among chip projects. 16, 8, 4, 2, 1 and ½ cycle cells can be used, for example. As is described above, each cell type has a preprogrammed output such as logic 1 or logic 0. Alternatively, cells that are not preprogrammed can be used, which are referred to herein as meta-connect cells (MCCEL). These MCCEL type cells are used to interconnect adjacent blocks of logic of an integrated circuit design and allow interconnect changes within any given metal interconnect layer of the integrated circuit. Data, control and/or radio frequency (RF) signals can be passed between adjacent logic blocks using the MCCEL according to the present invention.

[0223] [00117] FIG. 25 illustrates the general use of MCCELs according to the present invention. On an integrated circuit 2500, a first logic design block 2502 has neighboring logic design blocks 2504 and 2506, for example. MCCELs 2508 are used to interconnect logic design blocks 2504 and 2506 to block 2502. Additional logic design blocks located adjacent to logic design block 2502 can also be coupled thereto by additional MCCELs. Each MCCEL comprises any of the ladder structures described above. However, the ladder structures that form each MCCEL do are not coupled at M1 to power or ground, but provide electrical connectivity between one or more adjacent logic design blocks. An advantage

of this arrangement is that connections between adjacent logic design blocks can be modified during chip revisions at any metal or via layer, as described above in connection with the various MMCEL embodiments. Also, because of the complexity to today's integrated circuits, various logic design blocks are often developed by different design team within a company. According to this embodiment of the present invention, a standard approach is provided for connectivity between independently developed logic design blocks that are eventually laid-out adjacent to one another on an integrated circuit chip. A further benefit is yielded as design teams change from revision to revision, since the standard approach for connecting adjacent logic design blocks remains the same.

[0224] [00118] A block diagram of a single-line MCCEL 2600 is illustrated in FIG. 26A. A logic table corresponding to MCCEL 2600 is illustrated in FIG. 26B. MCCEL 2600 has a small footprint and accommodates a single layer metal change, according to the present invention. The MCCEL 2600 can undergo a limited number of metal changes as dictated by number of ladder "cycles" in a cell. The MCCEL 2600 has a single input and a single output, which can be tied to a logic '1', logic '0', or can be used as a connection to any metal layer as shown in the logic table of FIG. 26B. The MCCEL 2600 can be FIB'ed, buffered to reduce problems with long routes or heavy loads, and works with existing or new chip designs.

[0225] [00119] The MCCEL 2600 has the same basic architecture and layout as the single ladder MMCEL, but replaces the GND connection with an input "In" in the beginning of the ladder structure. This input "In" can be connected at any subsequent layer that is not yet utilized. The MCCEL 2600 can connect wires between logic blocks or can be used to break an existing connection to make a new one. Although the port names (i.e., the input and output) are uni-directional, the MCCEL 2600 is really bi-directional because it consists only of metal wires and metal vias. Thus, the electrical signal can readily propagate in both directions whether it is a pulse, static, or radio frequency (RF) signal.

[0226] [00120] An exemplary layout for a single-ladder MCCEL 2600 is illustrated in FIG. 27. An Input "In" is initially tied at Metal 1. Thereafter, other external sources can be connected to input "In" at any subsequent available metal layer. The MCCEL 2600 shares the same architecture and layout as the single ladder MMCEL described above (e.g., FIG. 3A), except for the initial GND connection in the beginning of the metal ladder.

[0227] [00121] Exemplary applications of the single-line MCCEL 2600 are illustrated in FIGs. 28A-28D.

[0228] [00122] FIG. 28A shows a default metal wire interconnection between a logic block 1 and a logic block 2 using two MCCELs. FIG. 28B shows a pull-up to VDD connection of logic block 2 using one MCCEL. The input to logic block 2 is now logic '1'. FIG. 28C shows a pull-down to GND connection of logic block 2 using one MCCEL. The input to logic block 2 is now logic '0'. FIG. 28D shows a new connection from another logic block to logic block 2 using one MCCEL. Logic block 2 is no longer connected to logic block 1.

[0229] [00123] The single-ladder version of single-line MCCEL has limited changes based on number of ladder "cycles" in the cell, as described above in connection with the single line-line MMCEL (e.g., FIGs. 2-3C).

[0230] [00124] A dual-line MCCEL 2900 is illustrated in FIG. 29A. A logic table corresponding to the dual-line MCCEL 2900 is illustrated in FIG. 29B. The dual-line MCCEL 2900 accommodates both single layer metal or single layer "via" changes, and an infinite number of changes on any single metal or "via" layer can be made per cell. Dual inputs terminals (I1 and I2) and dual outputs terminals (O1 and O2)are provided in each cell, with cross connect capability (i.e., the DPDT switch analogy described above applies). The dual-line MCCEL 2900 can be FIB'ed, it can be buffered to reduce problems with long routes or heavy loads, and it can be laid-out to fit within a standard cell library formats, as would become apparent to persons skilled in the relevant art. The dual-line MCCEL 2900 can be placed anywhere on the chip and works with existing or new chip designs. The dual-line MCCEL 2900 can be implemented using the same architecture and layout as the MMCEL described above, except VDD and GND are replaced with dual inputs.

[0231] [00125] Exemplary applications built with the dual-line MCCELs 2900, can include a: programmable DPDT logic switch; logic inverter; flip-flop output inverter; flip-flop set/clear selector; wired connector; universal I/O pad w/pull-up, pull-down, or no resistor options. Moreover, the MCCEL 2900 can be combined with the MMCEL to produce programmable unique logic functions, such as a universal I/O interface for logic blocks. MCCELs 2900 can be used for analog applications as well as digital applications. These examples are presented by way of example, not limitation.

[0232] [00126] Although the port names are uni-directional, the MCCEL 2900 is really bi-directional because it consists only of metal wires and metal vias. The electrical signal can readily propagate in both directions (whether propagating a pulse, static, or radio frequency (RF) signal). The default state of the MCCEL 2900 is entered whenever the number of MetalNia changes becomes even.

[0233] [00127] An exemplary default dual-line MCCEL 2900 is illustrated in FIG. 30. This layout comprises two metal ladders. Input signals In _1 and In_2 are tied at M1 of the metal ladder. Both ends of the metal ladder become the output signals of MCCEL 2900, such as Out_1 and Out_2. This layout structure is similar to the dual ladder MMCEL described above, except for the dual inputs.

[0234] [00128] FIG. 31 illustrates a layout change on

M5, as compared to M5 in FIG. 30, which is implemented using two cuts and two jumps.

[0235] [00129] The MCCEL 2900 can be combined with normal logic cells (e.g., inverters, nor, nand, flip-flops, etc.) to create programmable logic whose function can be modified by changing a single metal or via layer.

[0236] [00130] A dual-line MCCEL 2900 configured as a DPDT logic switch is illustrated in FIGS. 32A-32D.

[0237] [00131] FIG. 32A shows a programmable inverter 3202 having a MCCEL, which can invert the outputs of a logic function. A logic table corresponding to the programmable inverter 3202 is illustrated in FIG. 32B.

[0238] [00132] FIG. 32C shows a programmable flip-flop inverter 3204 having a MCCEL, which can swap the outputs of a flip flop without the need for an additional logic inverter. A logic table corresponding to the programmable flip-flop inverter 3204 is illustrated in FIG. 32D.

[0239] [00133] MCCELs can be embedded inside a logic gate of a library component to provide additional functionality as noted above. The MCCEL is well suited for specialized spare logic library cells called "spare cells".

[0240] **[00134]** An MCCEL can be configured to achieve the equivalent functionality to an MMCEL, as illustrated in FIG. 33A. A logic table corresponding to the MCCEL-MMCEL equivalent is illustrated in FIG. 33B. MCCEL 'I2' and 'I1' pins are tied directly to 'VDD' and 'GND', respectively, to emulate the same functionality of a MMCEL. However, the configuration shown in FIG. 33A is slightly larger than an MMCEL due to additional routing of the 'VDD' and GND' signals. Thus, it is recommend to use MMCEL if this type of functionality is required.

[0241] [00135] FIG. 33C shows an equivalent circuit to FIG. 33A. Series resistors (resistor) are placed between the 'VDD' or 'GND' and the 11 and 12 pins of the MCCEL to enable a weak pull-up or a weak pull-down. The weak pull-up or weak pull-down enables the MCCEL output pins 'O2' or 'O1' to be driven to a logic '1' or logic '0' if the signals 'In_2' and 'In_1' are not electrically driven (e.g., they are "floating"). If 'In_2' or 'In_1' are electrically driven, then the MCCEL will function according to its original design. The value of the weak pull-up or weak pull-down resistor is designed so that it does not interfere with the normal electrical function of the MCCEL. A buffer in series can be used to help drive high output fanouts. A logic table corresponding to the MCCEL-MMCEL equivalent in FIG. 33C is illustrated in FIG. 33D.

[0242] [00136] In one embodiment, MCCELs can be combined to perform unique logic functions such as the Programmable Flip-Flop Clear/Set Control logic (i.e., configured to control default register values), as shown on FIG. 34A. Two dual-line MCCELs (MCCEL1 and MCCEL2) are used to multiplex the appropriate 'reset' signal to either 'CLR' or 'SET' pins of a flip/flop. The MCCELs are connected in parallel.

[0243] **[00137]** If the 'RESET' signal is active low, then both 'Outl_2' and 'Out2_1' signals should be active low as well, and the 'GND' inputs to I1 of MCCEL1 and 12 of MCCEL2 should be tied to 'VDD'.

[0244] **[00138]** If 'RESET' is low, then 'Out2_1' and 'Outl_2' will be low because all inputs of the MCCELs are all low. The flip-flop should function normally based on its logic inputs.

[0245] **[00139]** If 'RESET' is high and both MCCELs are in its default state, then 'Out2_1' will be low and 'Out1_2' will be high. The 'CLR' pin will be high and the 'SET' pin will low. The flip-flop output gets cleared as shown on the Logic Table. The default state of the MCCELs is '0'.

[0246] **[00140]** If 'RESET' is high and both MCCELs are programmed to cross-connect, then 'Out2_1' will be high and 'Outl_2' will be low. The 'CLR' pin will be low and the 'SET' pin will high.

[0247] [00141] The flip-flop output is set as shown in FIG. 34B. MCCELs must be programmed at the same time, otherwise, the flip-flop will go into an indeterminate state because the 'CLR' and 'SET' inputs could both be high. The toggle state of the two MCCELs cannot be both a '1' and a '0'. MCCEL logic as shown in FIG. 34A performs its function without the need for any inverters or other logic gates. It is an all metal layer only solution which does not require any active silicon.

[0248] [00142] In another embodiment, MCCELs can also be combined to perform unique logic functions such as the Programmable Wire Connector logic shown in FIG. 35A. In FIG. 35A the MCCELs are connected in series . A logic table corresponding to FIG. 35A is illustrated in FIG. 35B. Two dual-line MCCELs are used to multiplex the appropriate pull-up resistor or pull-down resistor onto a wire carrying signal 'In2_2', which allows the wire carrying signal 'In2_2' to be effectively disconnected or connected from a wire carrying signal 'In2_1'. A feedback wire carrying signal 'Out2_2' enables the wire carrying signal 'In2_1' to remain connected to 'O2' of MCCEL2 after a metal or via change on MCCEL2.

[0249] **[00143]** If both MCCELs are in its default state, then 'Out2_1' will be coupled only to the wire carrying signal 'In2_1' as shown in FIG. 35A.

[0250] **[00144]** If MCCEL2 is programmed to cross-connect and MCCEL1 remains in its default condition, then 'Out2_1' will be coupled to the wires carrying signals 'In2_1' and 'In2_2' and a pull-down resistor.

[0251] **[00145]** If all of the wires carrying signals 'In2_2', 'In2_1', and 'Out2_1' are not driven but are kept floating, the state of all three wires will be a logic low because of the weak pull-down resistor.

[0252] **[00146]** If both MCCEL2 and MCCEL1 are programmed to cross-connect, then 'Out2_1' will be connected to the wires carrying signals 'In2_1' and 'In2_2' and a pull-up resistor.

[0253] **[00147]** If all of the wires carrying signals 'In2_2', 'In2_1', and 'Out2_1' are not driven but are kept

floating, the state of all three wires will be a logic high because of the weak pull-up resistor.

[0254] **[00148]** The value of the weak pull-up or weak pull-down resistor is designed so that it does not interfere with the normal electrical function of the wired connections. MCCEL1 is used to prevent floating nets. MMCEL1 is optional for the case where the wire carrying signal 'In2_2' is driven by the outputs of a logic cell. The MCCEL circuit of FIG. 35A performs the logic functions shown in FIG. 35B without the need for any inverters or other logic gates. It is an all metal layer only solution which does not require any active silicon.

[0255] [00149] In a still further embodiment, MCCELs can be combined to perform unique logic functions such as the Programmable I/O Pad Control logic shown in FIG. 36A. A logic table corresponding to FIG. 36A is illustrated in FIG. 36B. In FIG. 36A, the MCCELs are connected in series. Two dual-line MCCELs are used to multiplex the appropriate pull-up resistor, pull-down resistor, or no-resistor wire into the I/O pin's 'i/o_wire' that runs between the I/O pin and the I/O pad logic.

[0256] **[00150]** If both MCCELs are in its default state, then 'Out2_1' will be coupled to an open wire. The state of the 'i/o_wire' will follow the electrical signal that is driven on the I/O pin as shown on in FIG. 36B.

[0257] [00151] If the I/O pin is not driven but is kept floating, the state of the 'i/o_wire' will be indeterminate.

[0258] **[00152]** If MCCEL2 is programmed to cross-connect and MCCEL1 remains in its default condition, then 'Out2_1' will be coupled to a pull-down resistor. The state of the 'i/o_wire' will follow the electrical signal that is driven on the I/O pin. However, if the I/O pin is not driven but is kept floating, the state of the 'i/o_wire' will be a logic low because of the weak pull-down resistor.

[0259] **[00153]** If both MCCEL2 and MCCEL1 are programmed to cross-connect, then 'Out2_1' will be coupled to a pull-up resistor. The state of the 'i/o_wire' will follow the electrical signal that is driven on the I/O pin. However, if the I/O pin is not driven but is kept floating, the state of the 'i/o_wire' will be a logic high because of the weak pull-up resistor.

[0260] [00154] The value of the weak pull-up or weak pull-down resistor is designed so that it does not interfere with the normal electrical function of the I/O pad.

[0261] **[00155]** Above MCCEL logic as shown in FIG. 36A performs its function without the need for any inverters or other logic gates. It is an all metal layer only solution which does not require any active silicon.

[0262] [00156] In a still further embodiment, MCCELs can be combined to perform unique logic functions such as the Multi-Inputs Programmable Bi-Directional Multiplexer logic as shown in FIG 37. In FIG. 37, the MCCELs are connected in series. Multiple dual-line MCCELs are used to multiplex the appropriate inputs (Input 1 to N) to the outputs of the MCCEL output array. The smallest unit of this multiplex structure is basically a single MCCEL such as MCCEL1. This configuration is useful for selecting an output from a group of functional blocks to be driven as outputs of a MCCEL (Outl to OutN). All inputs can reach an output pin of an MCCEL, but it depends on the programmed state of the MCCEL (crossed or uncrossed). The multiplexer logic structure is non-blocking. There is no limitation on the type of electrical inputs to the MCCEL since its structure is basically a wire. The MCCEL logic performs its function without the need for any inverters or other logic gates. It is an all metal layer only solution which does not require any active silicon.

[0263] [00157] In a still further embodiment, MCCELs can be combined with MMCELs to perform unique logic functions such as the Programmable I/O Interface Control logic for interconnecting IP blocks as shown in FIG. 38A. A logic table corresponding to FIG. 38A is illustrated in FIG. 38B. The choices of interconnect for each input/output wire are logic '1', logic '0', or pass through connection. An MCCEL and an MMCEL are used to multiplex the appropriate 'VDD', 'GND', or 'In2_1' signals to 'Out2_1' and 'Out2_2'. The MMCEL is used to create the 'VDD' or 'GND' connection and the MCCEL is used to make the pass through connection to 'In2_1'. The MMCEL can be replaced by another MCCEL whose inputs are tied to series resistors instead of a direct connection to 'VDD' and 'GND'. This will prevent contention on the wire when the signals 'Out2_2' or 'Out2_1' are connected directly to an output pin on the logic block. This configuration with the MMCEL work when 'Out2_2' or 'Out2_1' are connected to input pins on the logic block. The two outputs 'Out2_1' and 'Out2_2' yield identical output conditions except for their starting default values. The appropriate output can be selected based on the desired starting default value as shown the logic table of FIG. 36B.

[0264] **[00158]** If MCCEL1 and MMCEL1 are in its default state, then 'Out2_1' will be coupled 'In2_1' and 'Out2_2' will be connected to logic '0'.

[0265] **[00159]** If MCCEL is programmed to cross-connect and MMCEL remains in its default condition, then 'Out2_1' will be coupled to logic '0' and 'Out2_2' will be coupled to 'In2_1'.

[0266] **[00160]** If MMCEL1 is programmed to cross-connect and MCCEL1 remains in its default condition, then 'Out2_1' will be coupled to 'In2_1' and 'Out2_2' will be coupled to a logic '0'.

[0267] **[00161]** If both MCCEL1 and MMCEL1 are programmed to cross-connect, then 'Out2_1' will be connected to a logic '1' and 'Out2_2' will be connected to a 'In2_1'.

[0268] [00162] The MCCEL logic shown in FIG. 38A performs its function without the need for any inverters or other logic gates. It is an all metal layer only solution that does not require any active silicon.

[0269] [00163] FIG. 39A illustrates a dual-line MCCEL for control of default register values according to the present invention. MCCELs can perform unique logic functions such as the programmable flip-flop clear/set control logic shown in this figure. In this embodiment, a

dual-line MCCEL is used to multiplex the appropriate active high 'RESET' signal to either the 'CLR' or 'SET' active high pins of the flip-flop. Based on the state of the MCCEL, the flip-flop can either be cleared or set when the reset is active. If 'RESET' is low, the outputs of MCCEL1 will always be low. Both 'CLR' and 'SET' pins of the flip-flop will be low. The output 'Reg_Q' of the flip-flop will follow its input 'In' on the rising edge of the clock signal 'CLK'. If 'RESET' is high and MCCEL1 is in its default state of '0' (uncrossed), then 'Outl_1' will be low and Outl_2 will be high. The 'CLR' pin will be high and the 'SET' pin will low. The flip-flop output is cleared as shown in the accompanying logic table of FIG. 39B. If 'RESET' is high and MCCEL1 is in state '1' (crossed), then 'Out1_1' will be high and Outl_2 will be low. The 'CLR' pin will be low and the 'SET' pin will high. The flip-flop output is set as shown in the logic table. If the 'RESET' signal is active low, then both 'CLR' and 'SET' signals should also be active low and the 'GND' inputs to I1 of MCCEL1 should be tied to 'VDD' instead. The MCCEL logic as shown in FIG. 39A performs its function without the need for any inverters or other logic gates. It is an all-metal layer only solution that does not require any active silicon.

Conclusion

[0270] [00164] Consequently, embodiments of the present invention provide at least the following advantages as compared to conventional methodologies: reduces additional metal mask costs due to revision ID, default register changes or connectivity between adjacent blocks of logic; reduces additional labor costs due to implementation of above features; the metal layer only implementation reduces the costs and complexity of implementation; single metal layer or via layer changes can be made at any metal layer; provides unlimited modification capability; a small footprint size saves area on the chip; excellent reliability due to metal only implementation; dual output per cell, logic 1 and logic 0, eliminates need for inverters and buffers; fits in standard cell format which simplifies layout; can be physically FIB etched to change defaults after chip has been manufactured; can be placed anywhere on the chip to reduce routing congestion; can be implemented in existing or new chip designs; does not introduce Design Rule Check (DRC) and Layout vs. Schematic Check (LVS) errors in layout such as floating metal after changing a metal or a via layer; requires power and ground only on M1, which improves route ability and reduces blockage; and can be used to customize unique customer specific requirements by reprogramming default registers.

[0271] [00165] While various embodiments of the present invention have been described above, it should be understood that they have been presented by way of example only, and not limitation. It will be apparent to persons skilled in the relevant art that various changes in form and detail can be made therein without departing from the spirit and scope of the invention. Thus, the breadth and scope of the present invention should not be limited by any of the above-described exemplary embodiments, but should be defined only in accordance with the following claims and their equivalents.

Claims

1. In an integrated circuit chip including a plurality of metal layers and first and second supply potentials, a programmable memory cell for storing a value, the memory cell comprising:

   a first metal interconnect structure that traverses the plurality of metal layers using a first plurality of vias;
   a second metal interconnect structure that traverses the plurality of metal layers using a second plurality of vias, wherein prior to programming, said first and second metal interconnect structures are coupled at a top metal layer; and
   an output coupled to one of the first and second supply potentials by at least one of said first and second metal interconnect structures, wherein a state of said output is programmable by altering at least one of the plurality of metal layers.

2. The memory cell of claim 1, further comprising multiples of said first and second metal interconnect structures coupled together to form a plurality of programmable cycles for the memory cell, wherein each half cycle is programmable at least once.

3. The memory cell of claim 2, wherein one cycle is laid out to form a ladder structure that traverses the plurality of metal layers from a bottom metal layer to a top metal layer and back to the bottom metal layer.

4. In an integrated circuit chip including a plurality of metal layers and first and second supply potentials, a programmable memory cell for storing a value, the memory cell comprising:

   a first metal interconnect structure that traverses the plurality of metal layers using a first plurality of vias;
   a second metal interconnect structure that traverses the plurality of metal layers using a second plurality of vias,
   an output coupled to one of the first and second supply potentials by at least one of said first and second metal interconnect structures, wherein each of said first and second metal interconnect structures can be programmed repeatedly by altering any one of the plurality of metal layers

and any one of a plurality of via layers.

5. The memory cell of claim 4, wherein said first and second metal interconnect structures are not electrically coupled to each other at a top metal layer thereby forming two outputs for the memory cell.

6. In an integrated circuit chip including first and second supply potentials, a method of making a programmable memory cell for storing a value, the method comprising:

forming a plurality of metal layers separated by a plurality of via layers;
forming a first metal interconnect structure that traverses the plurality of metal layers using a first plurality of vias in the plurality of via layers;
forming a second metal interconnect structure that traverses the plurality of metal layers using a second plurality of vias in the plurality of via layers;
coupling together said first and second metal interconnect structures at a top metal layer prior to programming;
coupling one of the first and second supply potentials to at least one of said first and second metal interconnect structures to form an output; and
altering at least one of the plurality of metal layers to thereby program the output.

7. The method of claim 6, further comprising forming multiples of the first and second metal interconnect structures and coupling together the first and second metal interconnect structures to form a plurality of programmable cycles for the memory cell, wherein each half cycle is programmable at least once.

8. In an integrated circuit chip including first and second supply potentials, a method of making a programmable memory cell for storing a value, the method comprising:

forming a plurality of metal layers separated by a plurality of via layers;
forming a first metal interconnect structure that traverses the plurality of metal layers using a first plurality of vias in the plurality of via layers;
forming a second metal interconnect structure that traverses the plurality of metal layers using a second plurality of vias in the plurality of via layers;
coupling together said first and second metal interconnect structures at a top metal layer prior to programming;
coupling the first supply potential to the first interconnect structure and the and second supply potential to the second interconnect structure to form two outputs; and
altering at least one of the plurality of metal layers to thereby program at least one of the outputs.

9. In an integrated circuit chip including a plurality of metal layers and first and second supply potentials, a memory cell circuit for modification of a default register value, the circuit comprising:

a memory cell having
a first metal interconnect structure that traverses the plurality of metal layers using a first plurality of vias, wherein said first metal interconnect structure is coupled to one of said first and second supply potentials,
a second metal interconnect structure that traverses the plurality of metal layers using a second plurality of vias, wherein said second metal interconnect structure is coupled to the other one of said first and second supply potentials, and
an output, wherein a state of said output is programmable by altering any one of the plurality of metal layers or any one of a plurality of via layers;
a register having a data input, a data output and control inputs; and
a control circuit coupled to said control inputs of said register, wherein said control circuit receives a chip reset signal and said memory cell output to thereby force said data output of said register to a default register value that equals said output of said memory cell, regardless of said data input of said register.

10. In an integrated circuit chip including a plurality of metal layers, first and second supply potentials and at least two adjacent logic blocks, a modifiable circuit for coupling the at least two adjacent logic blocks, comprising:

a first metal interconnect structure that traverses the plurality of metal layers using a first plurality of vias, wherein said first metal interconnect structure is located at a boundary of the at least two adjacent logic blocks;
a second metal interconnect structure that traverses the plurality of metal layers using a second plurality of vias, wherein said second metal interconnect structure is located at said boundary of the at least two adjacent logic blocks; and
an interconnect formed between the at least two adjacent logic blocks by at least one of said first and second metal interconnect structures, wherein a state of said interconnect is programmable by altering any one of the plurality of met-

al layers or any one of a plurality of via layers.

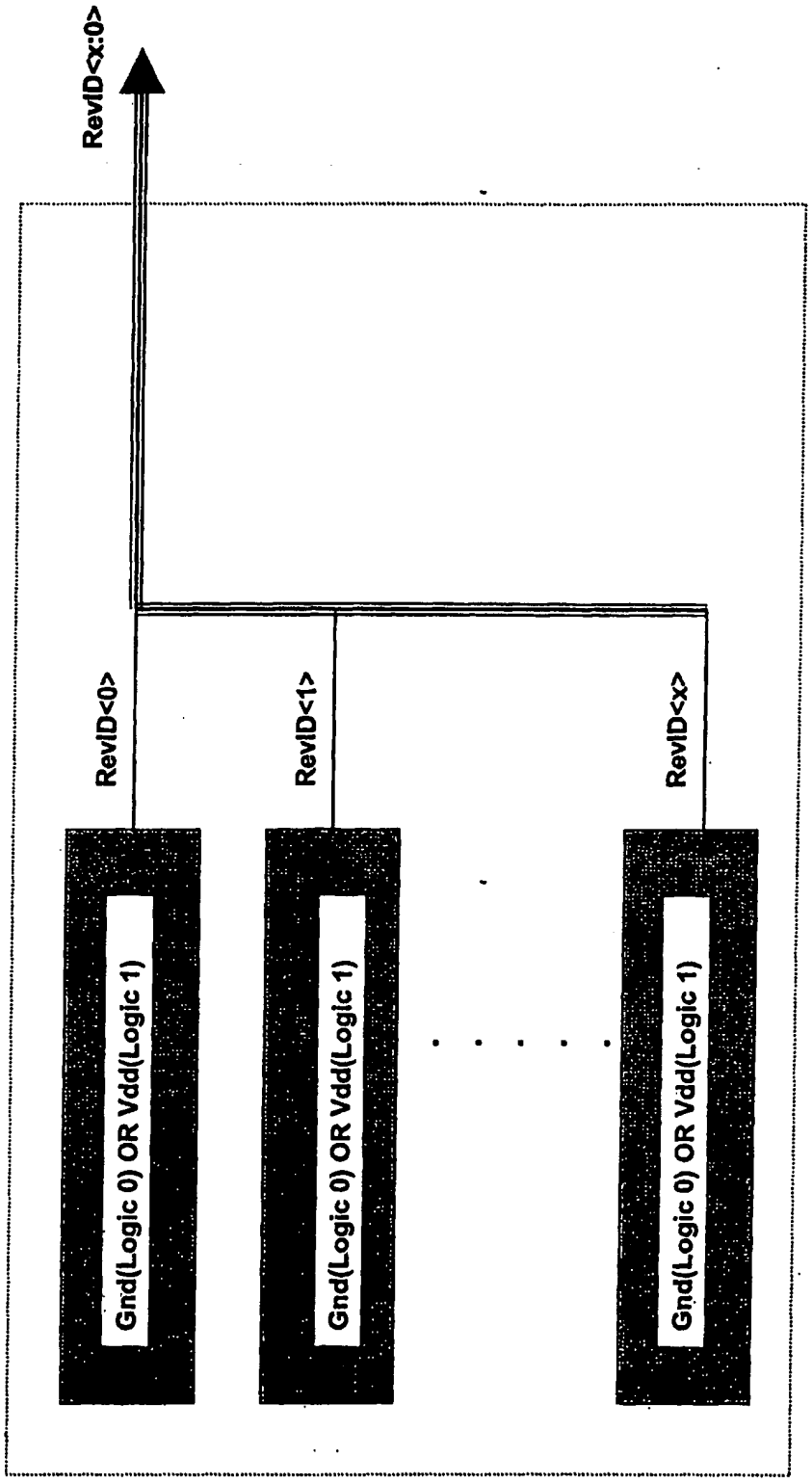

RevID<x:0>
RevID<0>
RevID<1>
RevID<x>
Gnd(Logic 0) OR Vdd(Logic 1)
Gnd(Logic 0) OR Vdd(Logic 1)
Gnd(Logic 0) OR Vdd(Logic 1)

FIG. 1

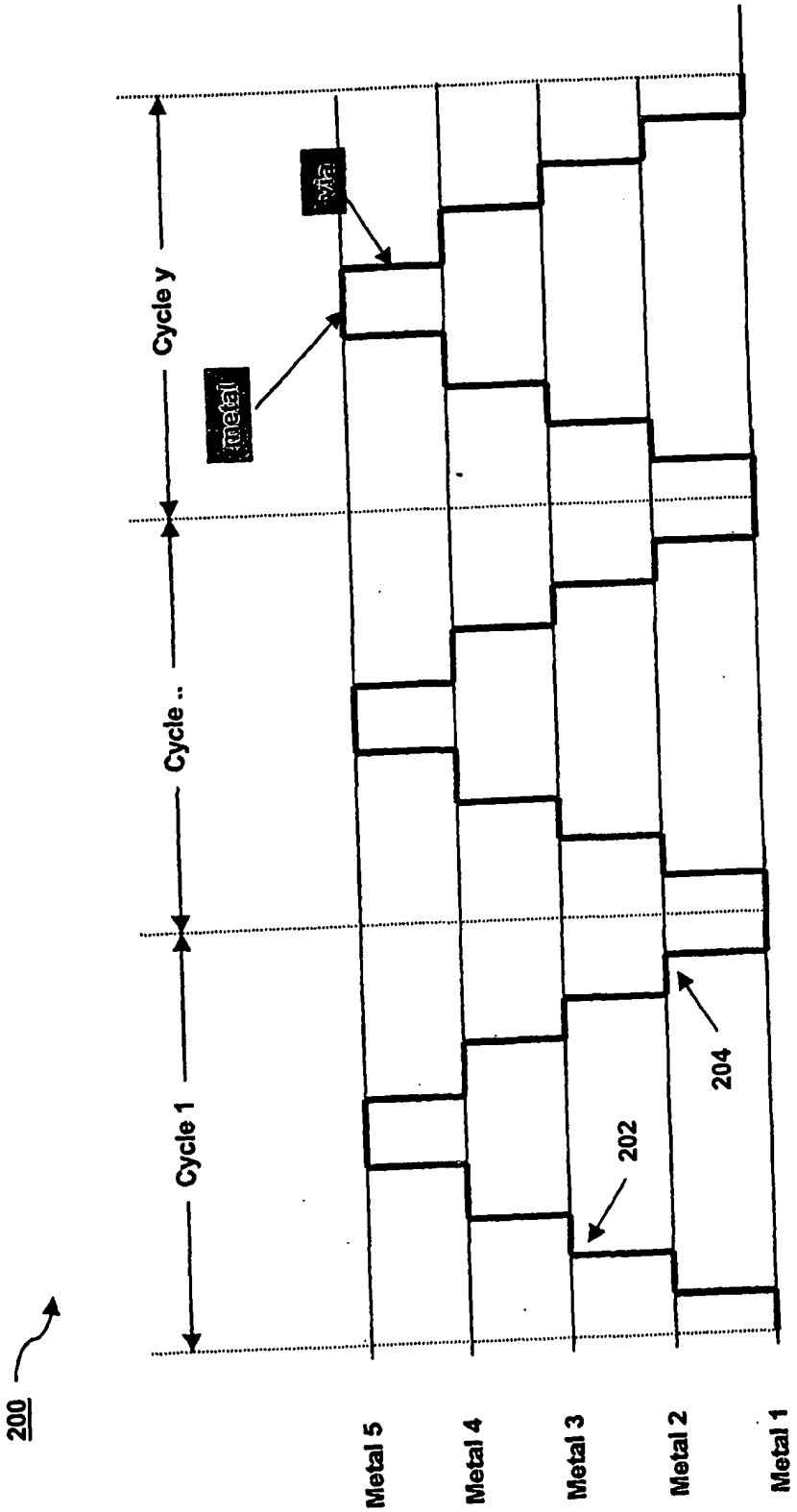

200
Cycle 1
Cycle ..
Cycle y
metal
Metal 5
Metal 4
Metal 3
Metal 2
Metal 1
202
204

FIG. 2

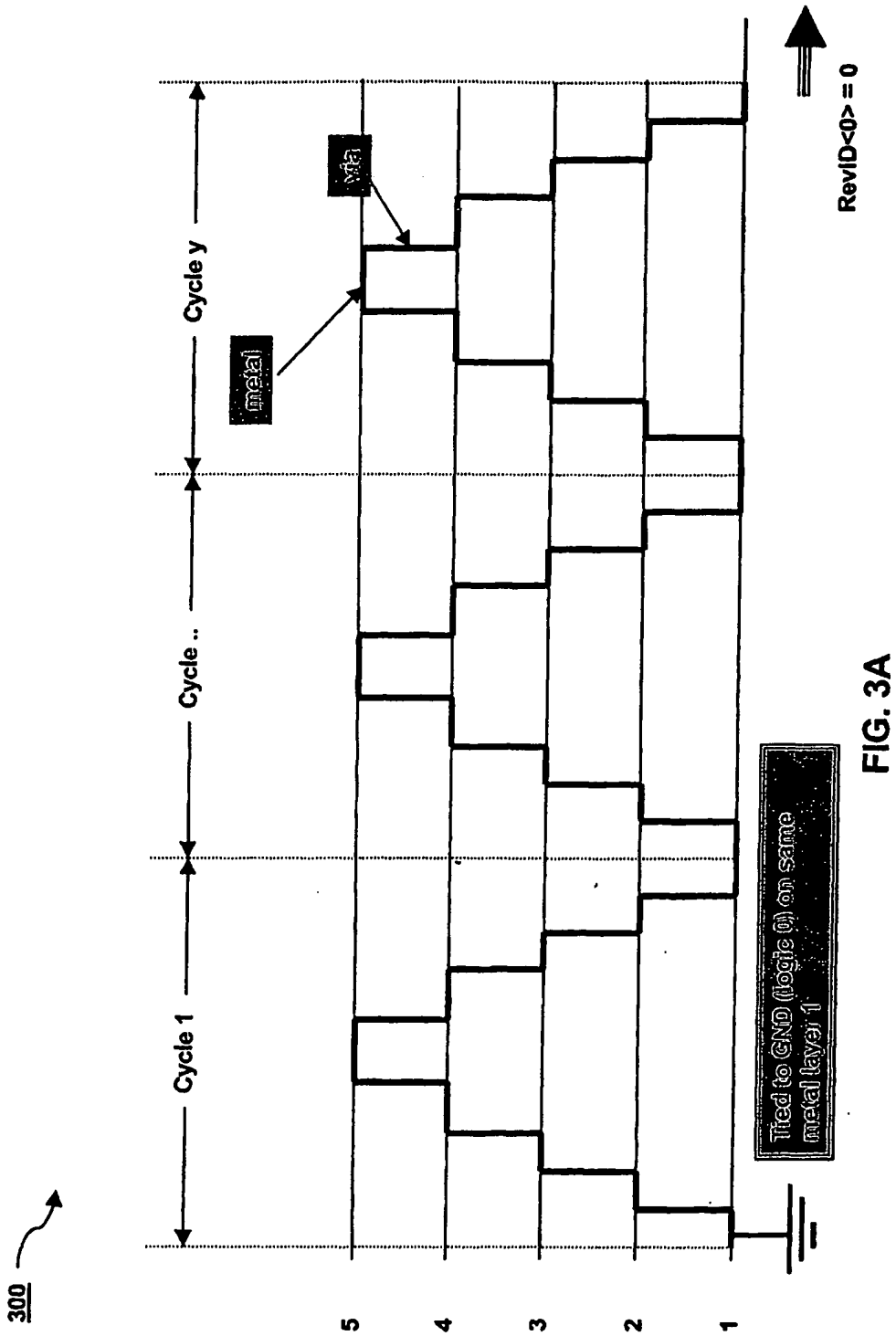

300
Cycle 1
Cycle ..
Cycle y
metal
via
Metal 5
Metal 4
Metal 3
Metal 2
Metal 1
Tied to GND (logic 0) on same metal layer 1
RevID<0> = 0

FIG. 3A

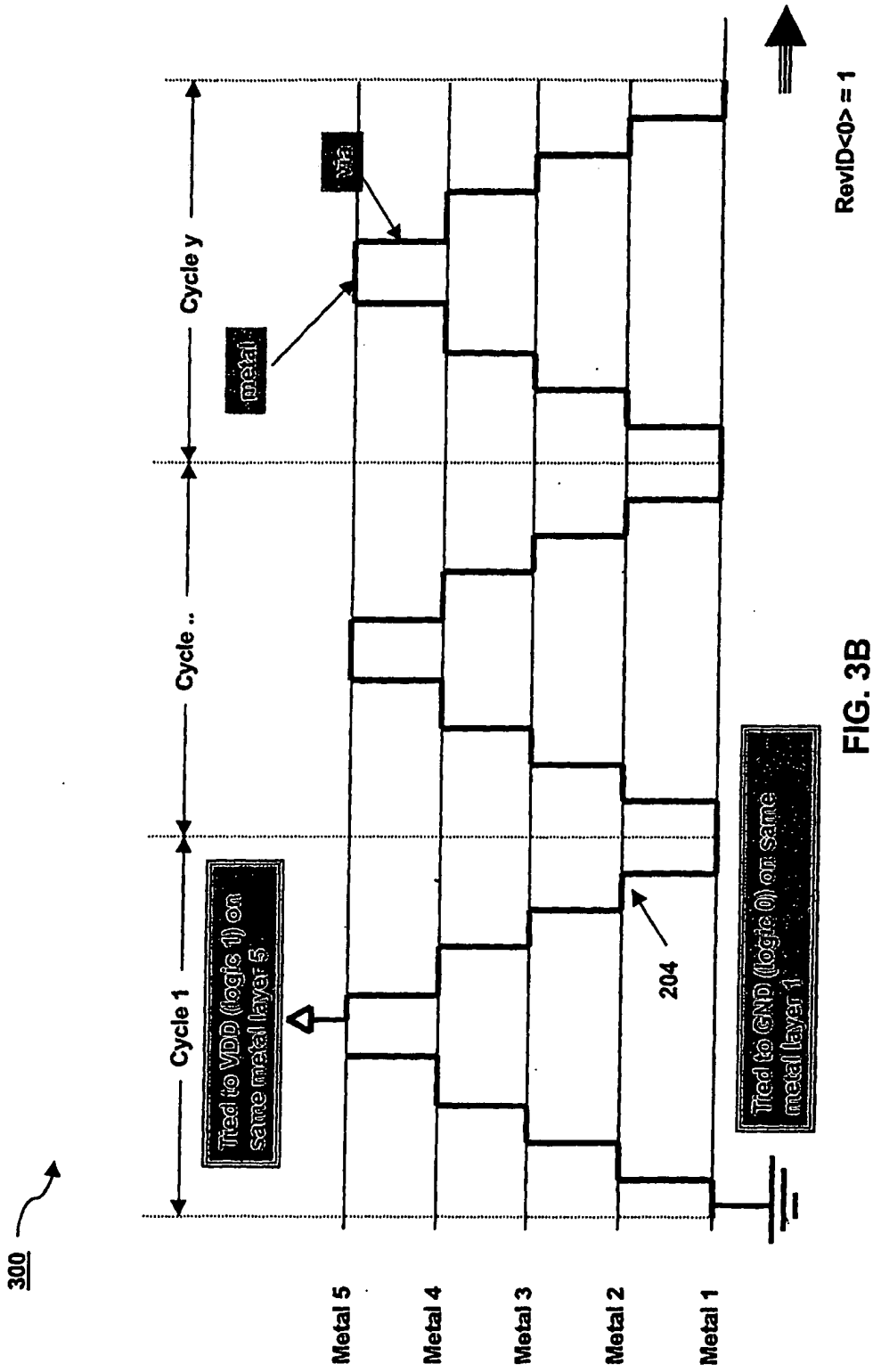

300
Cycle 1
Cycle ..
Cycle y
Tied to VDD (logic 1) on same metal layer 5
Via
metal
204
Tied to GND (logic 0) on same metal layer 1
RevID<0> = 1
Metal 5
Metal 4
Metal 3
Metal 2
Metal 1

FIG. 3B

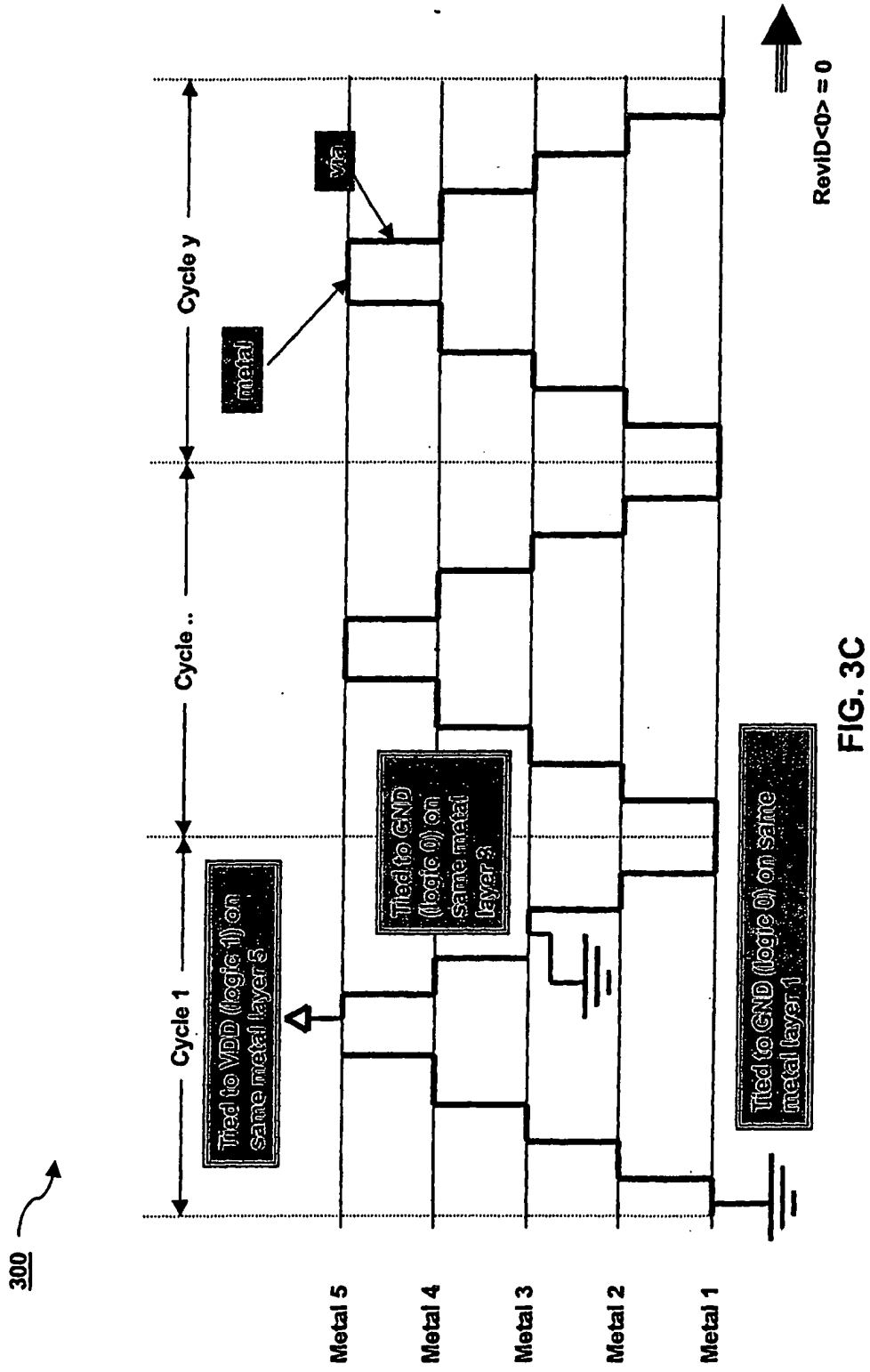

300
Cycle 1
Cycle ..
Cycle y
Tied to VDD (logic 1) on same metal layer 5
Tied to GND (logic 0) on same metal layer 3
Tied to GND (logic 0) on same metal layer 1
metal
via
RevID<0> = 0
Metal 5
Metal 4
Metal 3
Metal 2
Metal 1

FIG. 3C

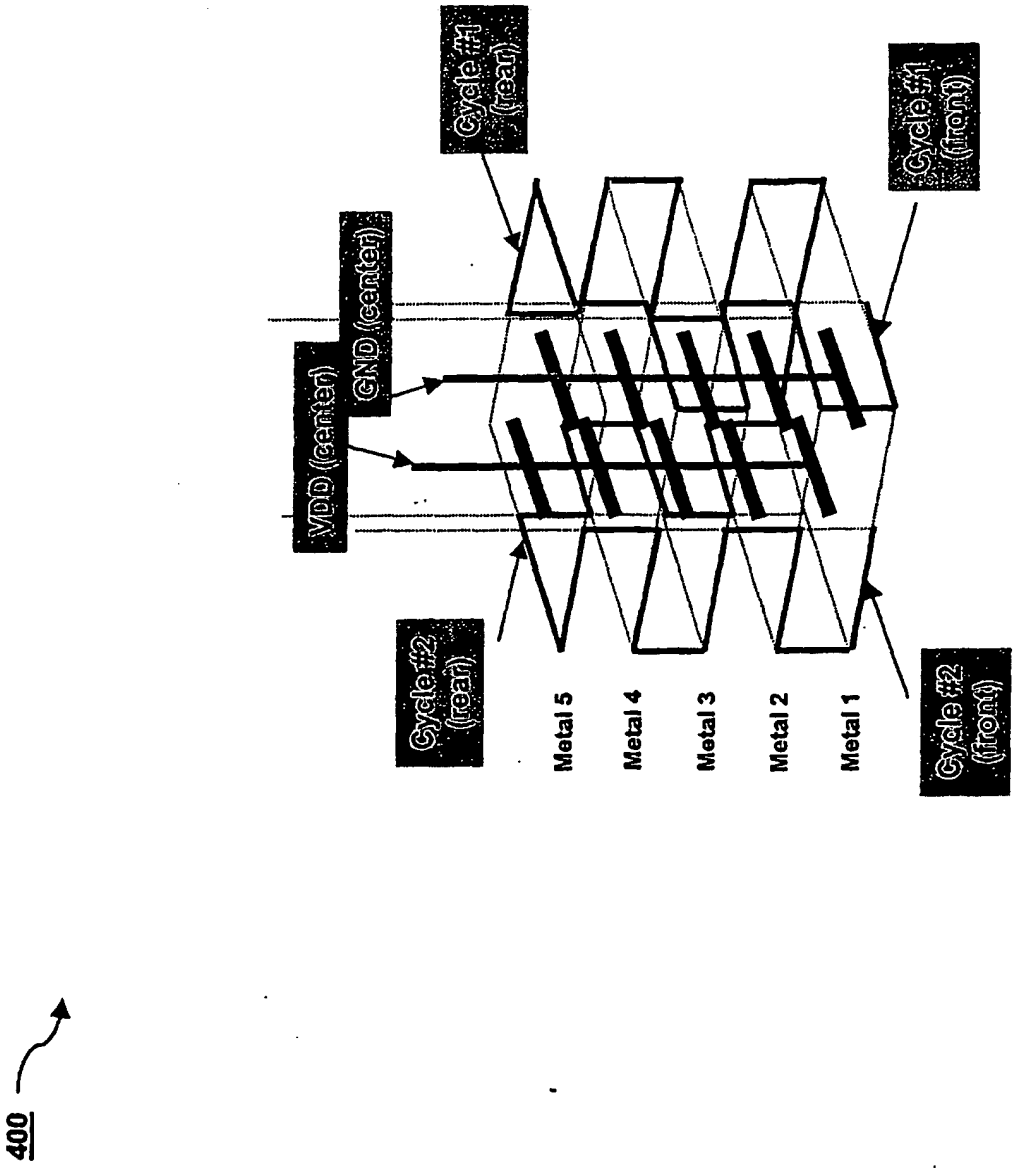

Cycle #1 (rear)
Cycle #1 (front)
VDD (center)
GND (center)
Cycle #2 (rear)
Cycle #2 (front)
Metal 5
Metal 4
Metal 3
Metal 2
Metal 1
400

FIG. 4

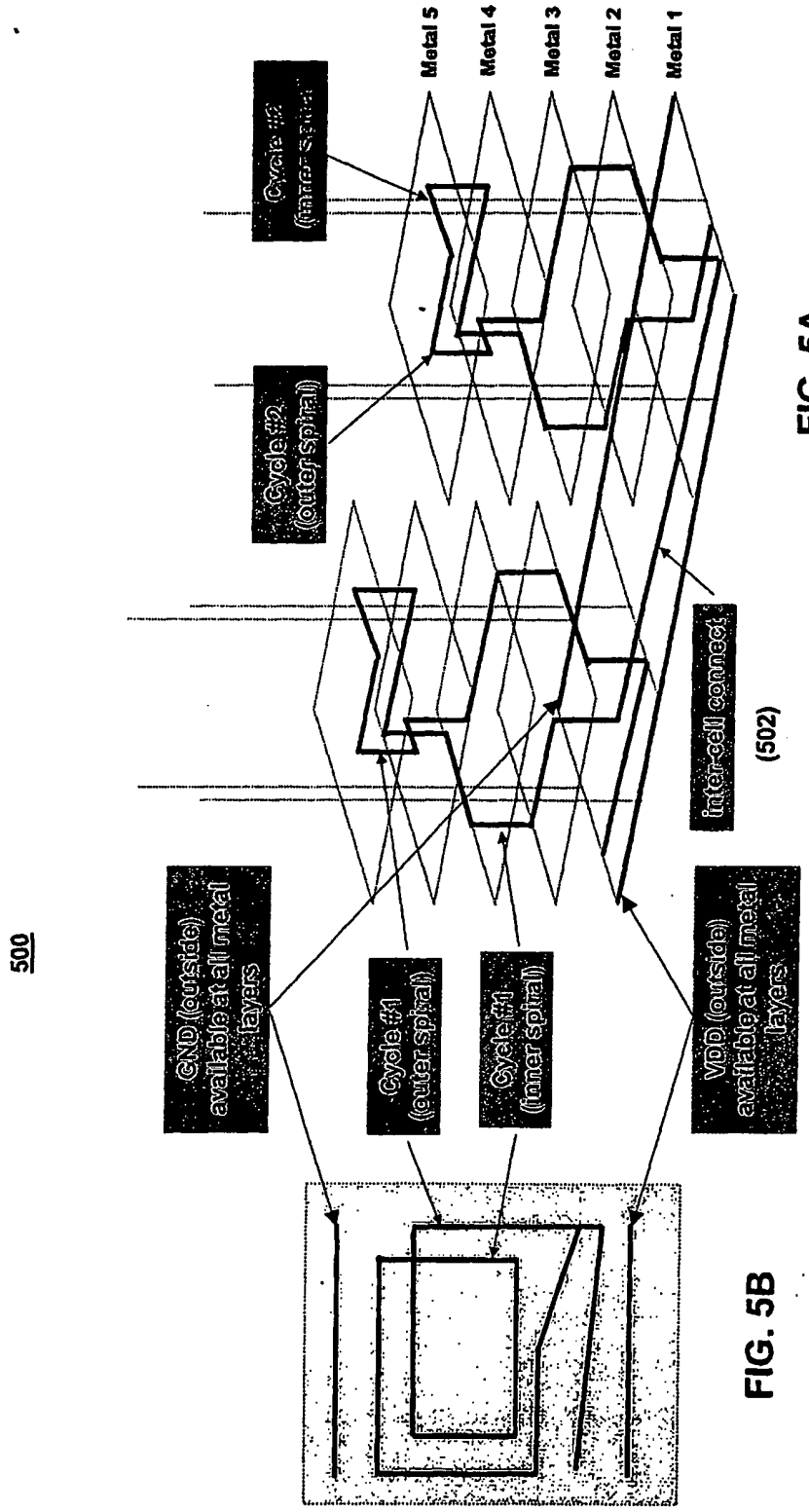

500
Metal 5
Metal 4
Metal 3
Metal 2
Metal 1
Cycle #2 (outer spiral)
inter-cell connect
(502)
GND (outside) available at all metal layers
Cycle #1 (outer spiral)
Cycle #1 (inner spiral)
VDD (outside) available at all metal layers

FIG. 5A

FIG. 5B

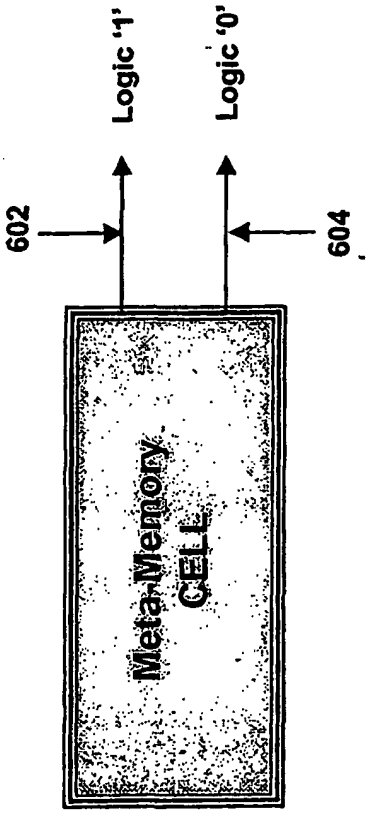


FIG. 6

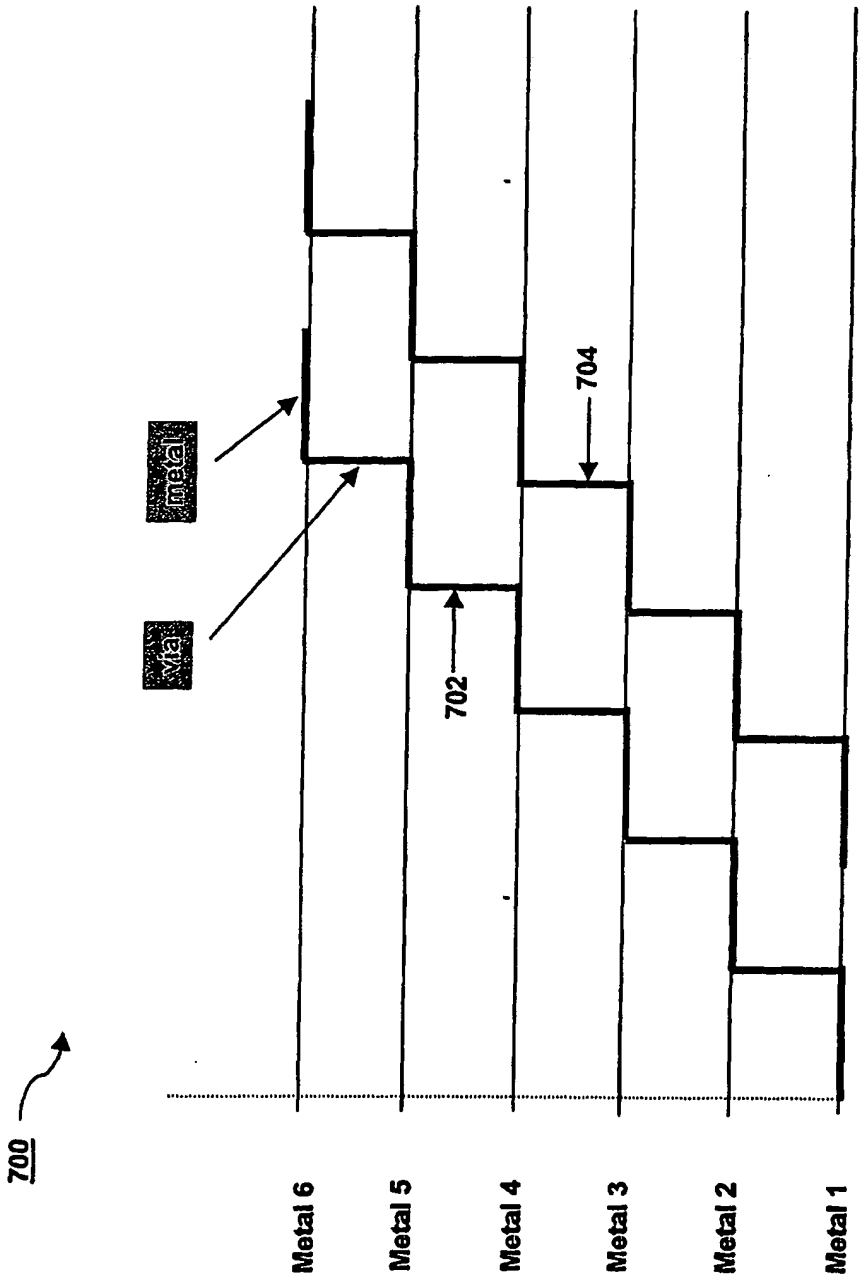

700
metal
via
702
704
Metal 6
Metal 5
Metal 4
Metal 3
Metal 2
Metal 1

FIG. 7A

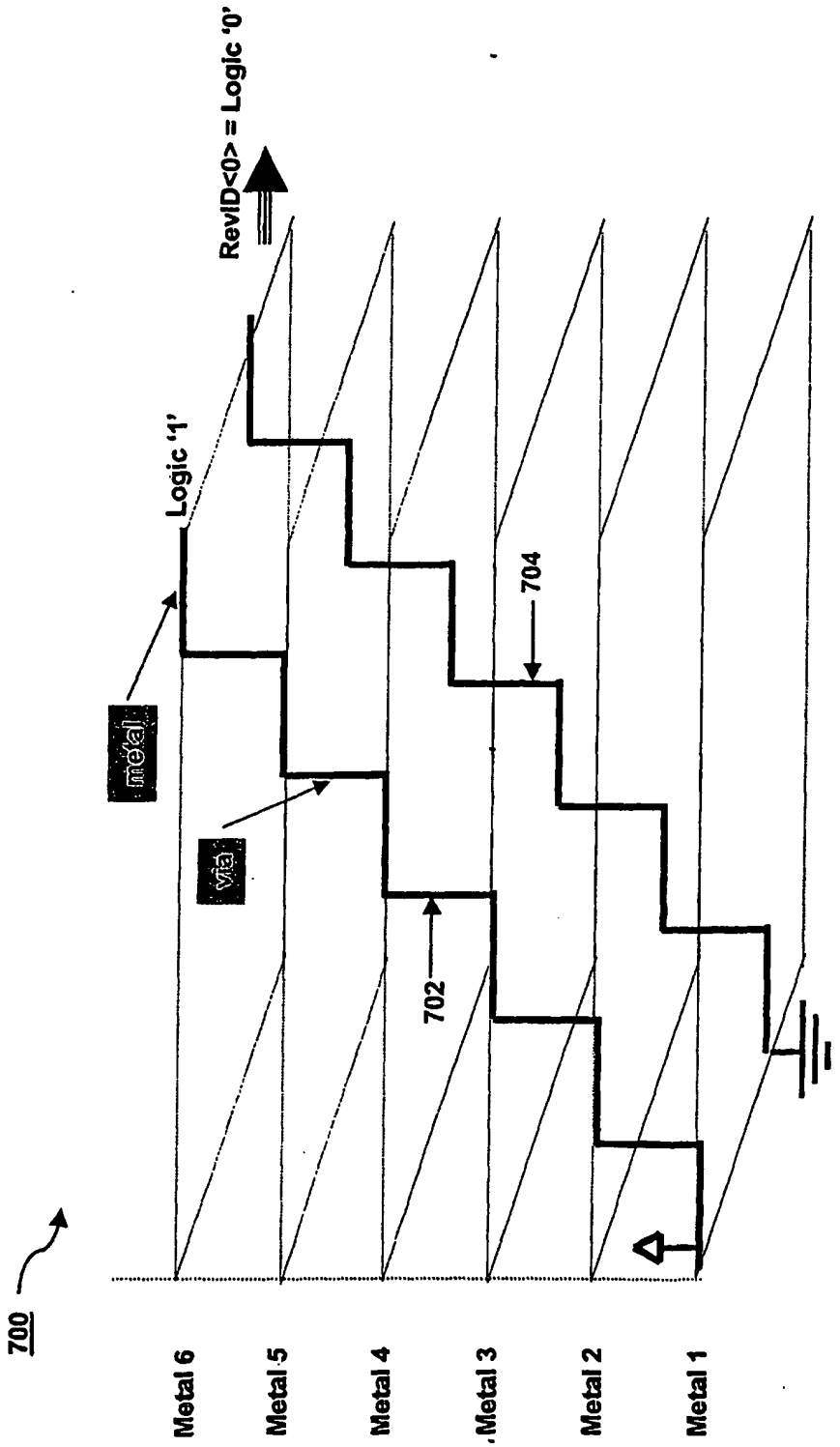

RevID<0> = Logic '0'
Logic '1'
metal
via
704
702
700
Metal 6
Metal 5
Metal 4
Metal 3
Metal 2
Metal 1

FIG. 7B

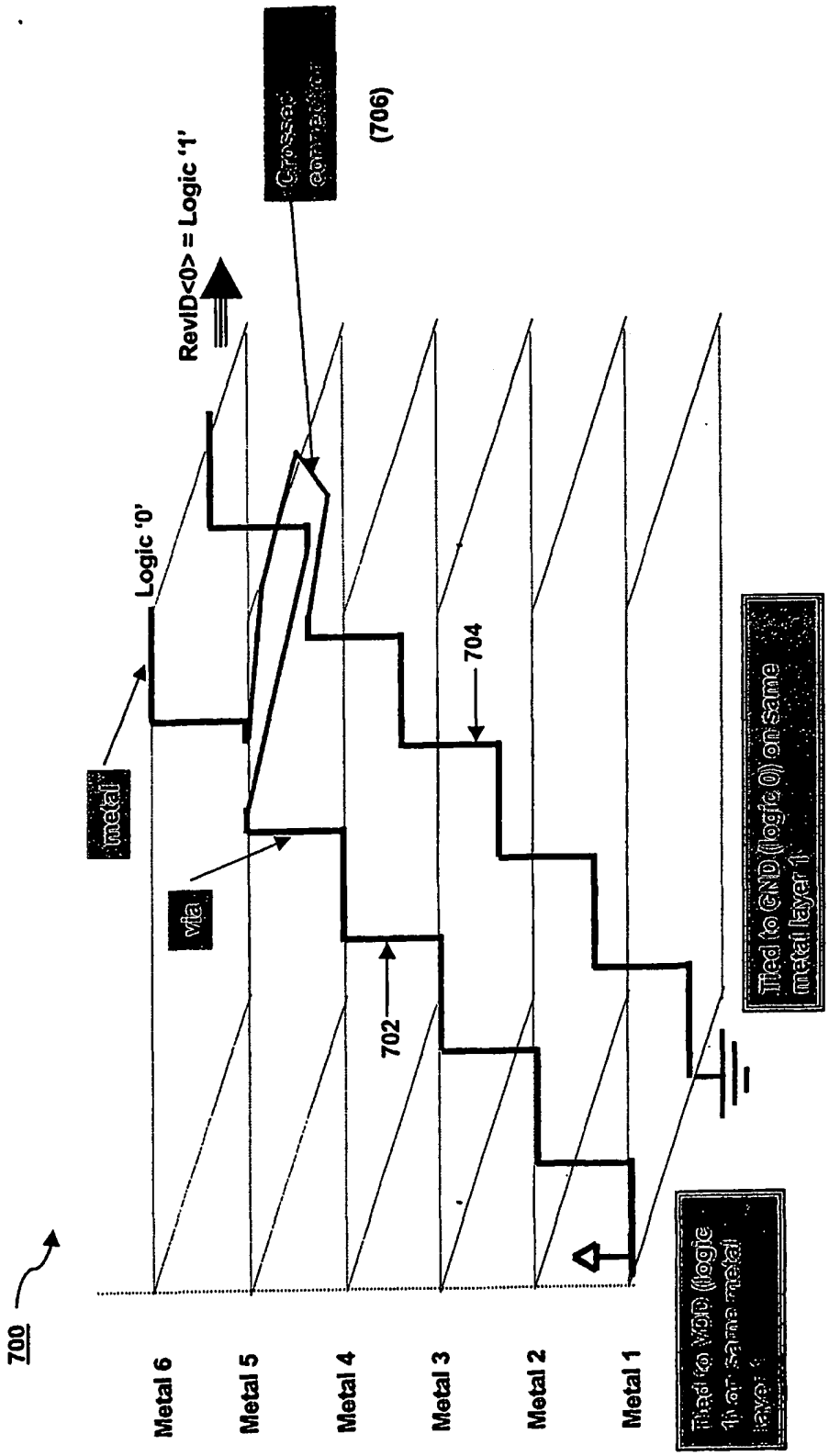

700
Metal 6
Metal 5
Metal 4
Metal 3
Metal 2
Metal 1
Tied to VDD (logic 1) on same metal layer
Tied to GND (logic 0) on same metal layer 1
RevID<0> = Logic '1'
Logic '0'
Crossed connection
(706)
metal
via
702
704

FIG. 7C

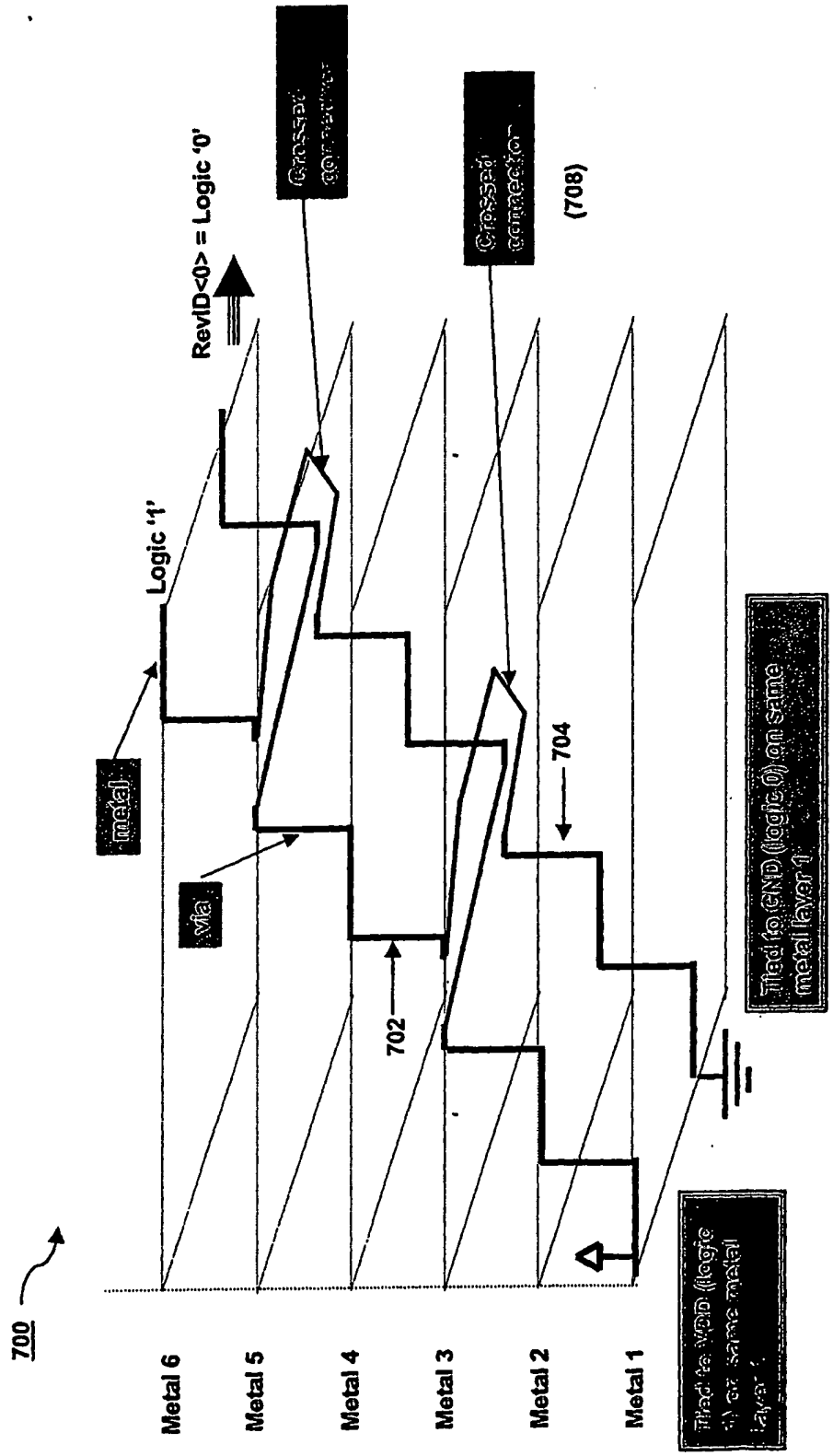

700
Metal 6
Metal 5
Metal 4
Metal 3
Metal 2
Metal 1
Tied to VDD (logic 1) on same metal layer
Tied to GND (logic 0) on same metal layer 1
RevID<0> = Logic '0'
Logic '1'
metal
Via
Crossed connection
Crossed connection
(708)
702
704

FIG. 7D

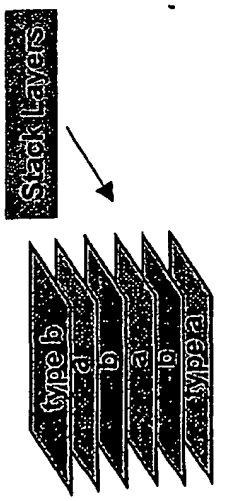

Stack Layers
type b
type a
type a
type a
type a

FIG. 8A

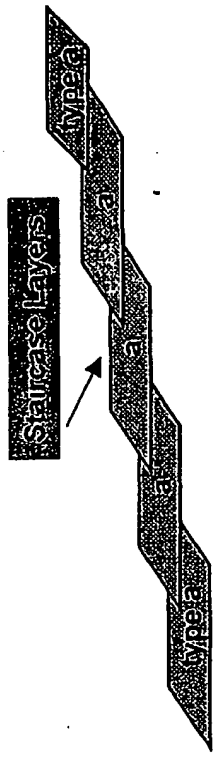

Staircase Layers
type a
type a
type a
type a
type a

FIG. 8B

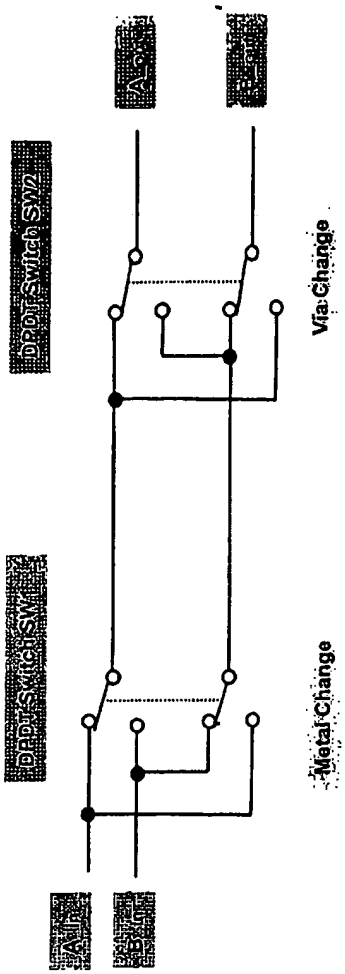

A out
B out
DPDT Switch SW2
Via Change
DPDT Switch SW1
Metal Change
A in
B in

FIG. 9B

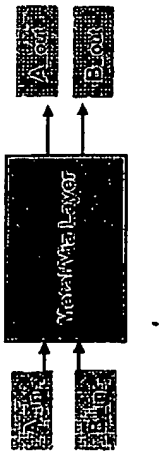

A out
B out
Metal/Via Layer
A in
B in

FIG. 9A

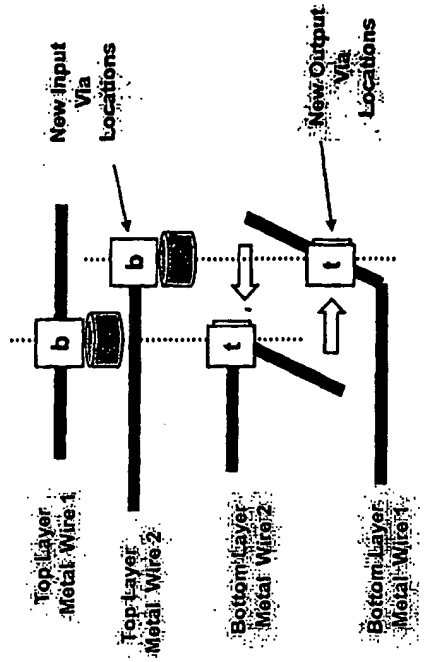
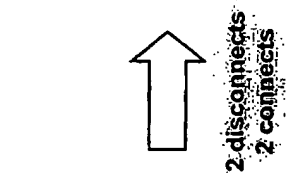

New Input Via Locations
New Output Via Locations
b
t
Top Layer Metal Wire 1
Top Layer Metal Wire 2
Bottom Layer Metal Wire 2
Bottom Layer Metal Wire 1

FIG. 9D


2 disconnects
2 connects

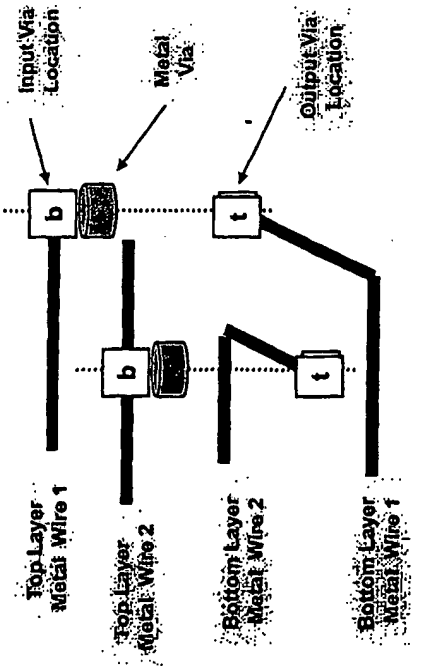

Input Via Location
Metal Via
Output Via Location
b
t
Top Layer Metal Wire 1
Top Layer Metal Wire 2
Bottom Layer Metal Wire 2
Bottom Layer Metal Wire 1

FIG. 9C

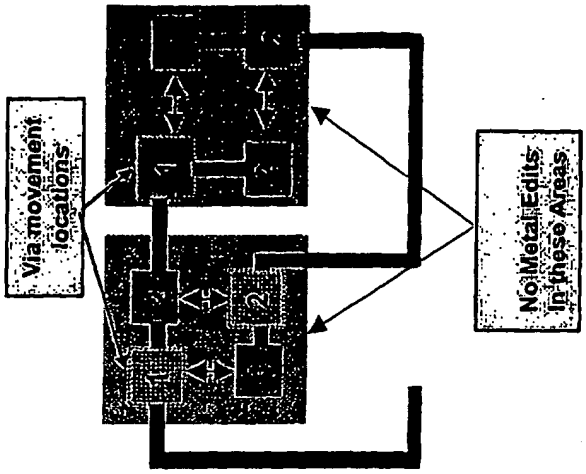


FIG. 10B

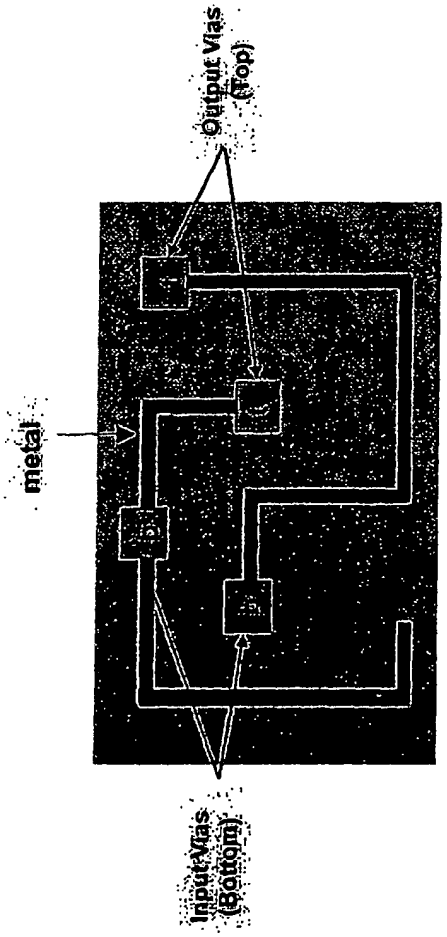


FIG. 10A

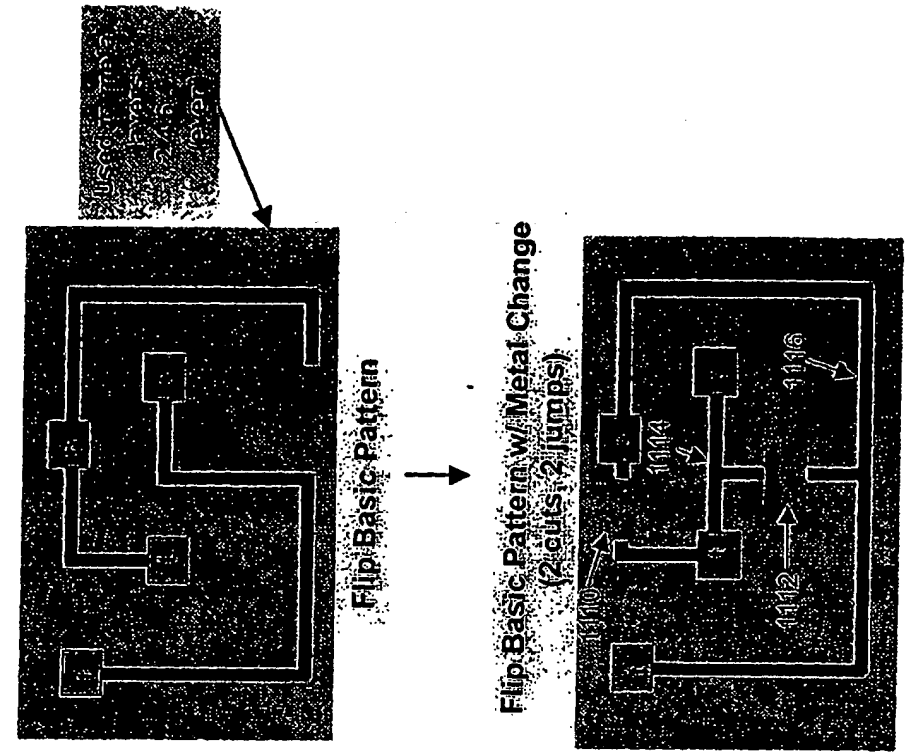


FIG. 11C

FIG. 11D

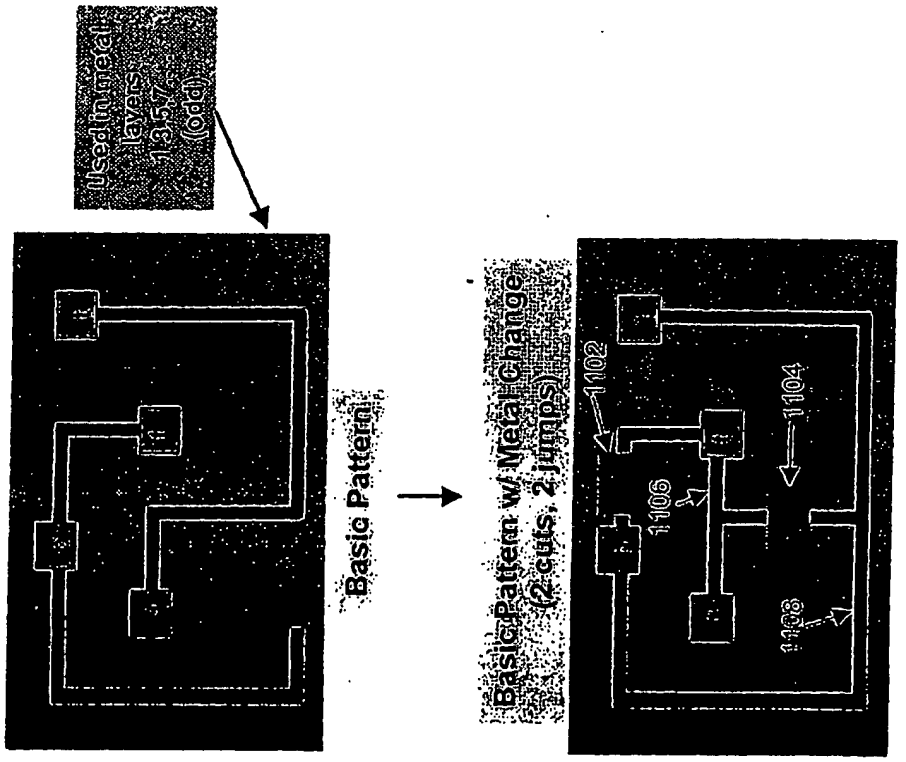


FIG. 11A

FIG. 11B

FIG. 12A

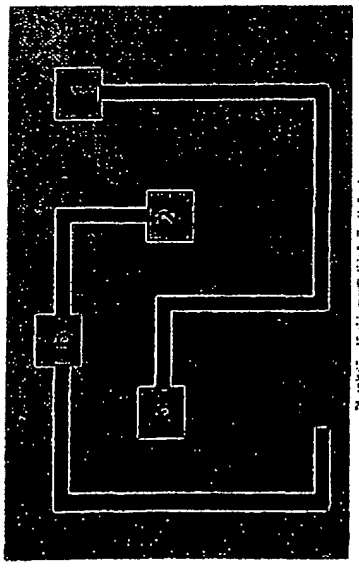


FIG. 12B

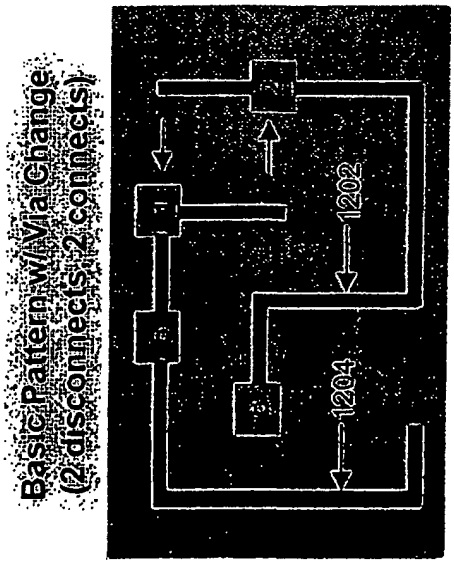


FIG. 12C

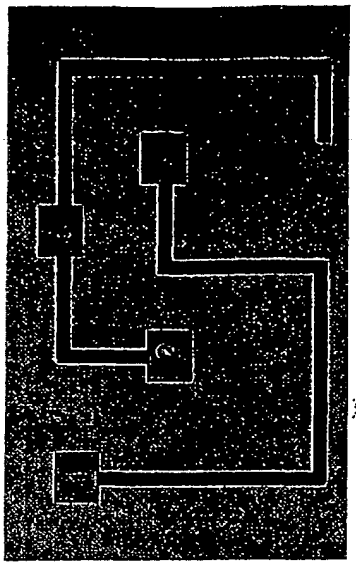
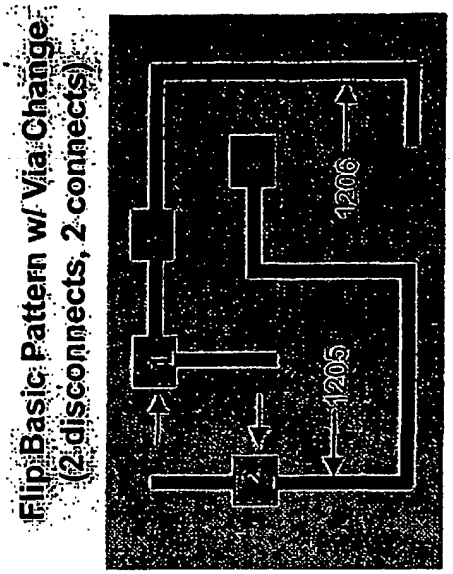


FIG. 12D



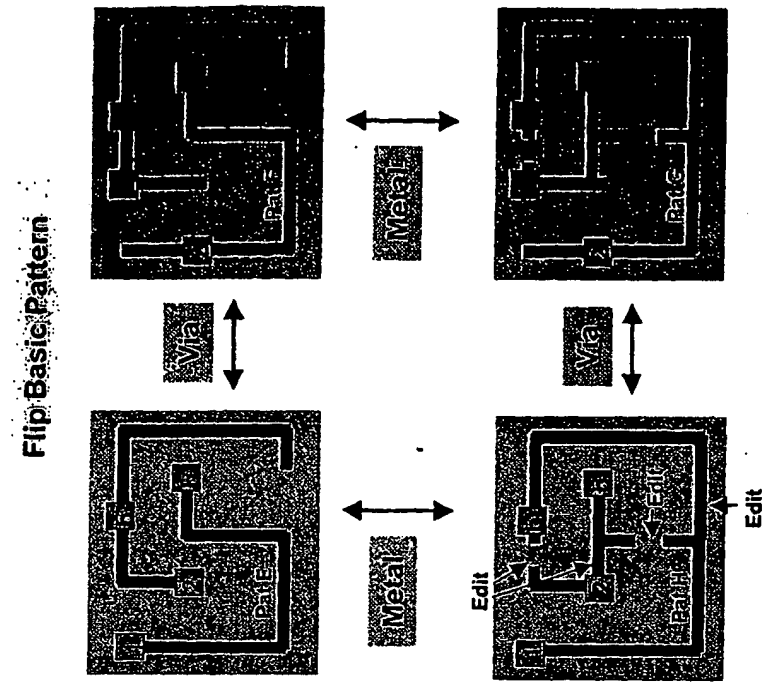

Flip Basic Pattern
Via
Metal
Via
Metal
Edit
Edit
Edit
Edit

FIG. 14

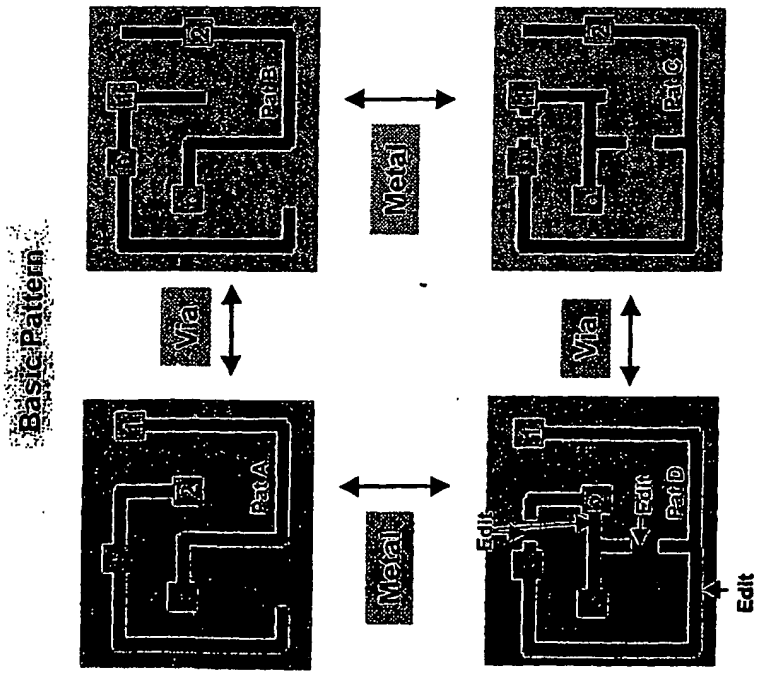

Basic Pattern
Via
Metal
Via
Metal
Edit
Edit
Edit
Edit

FIG. 13

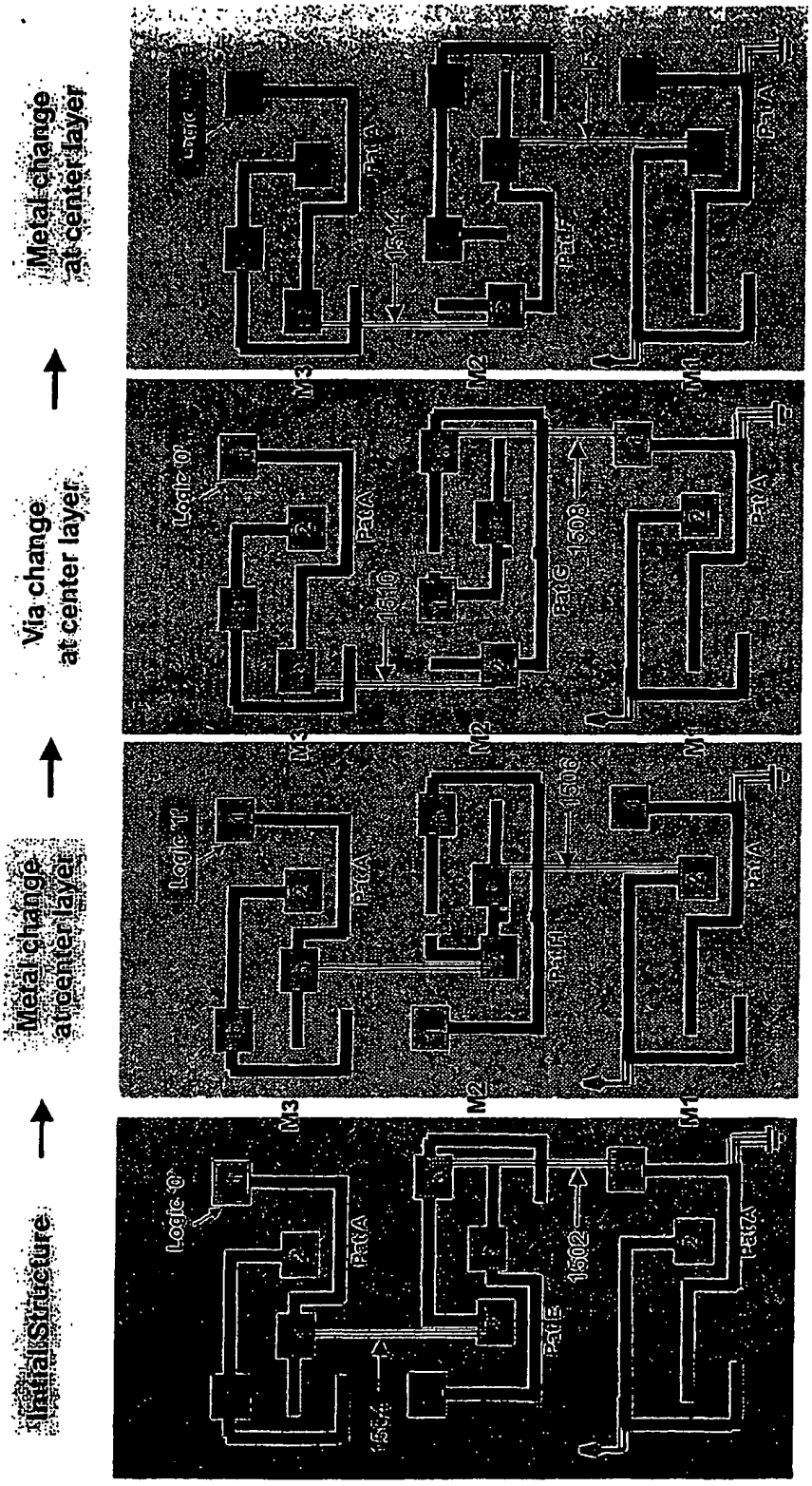


FIG. 15A FIG. 15B FIG. 15C FIG. 15D

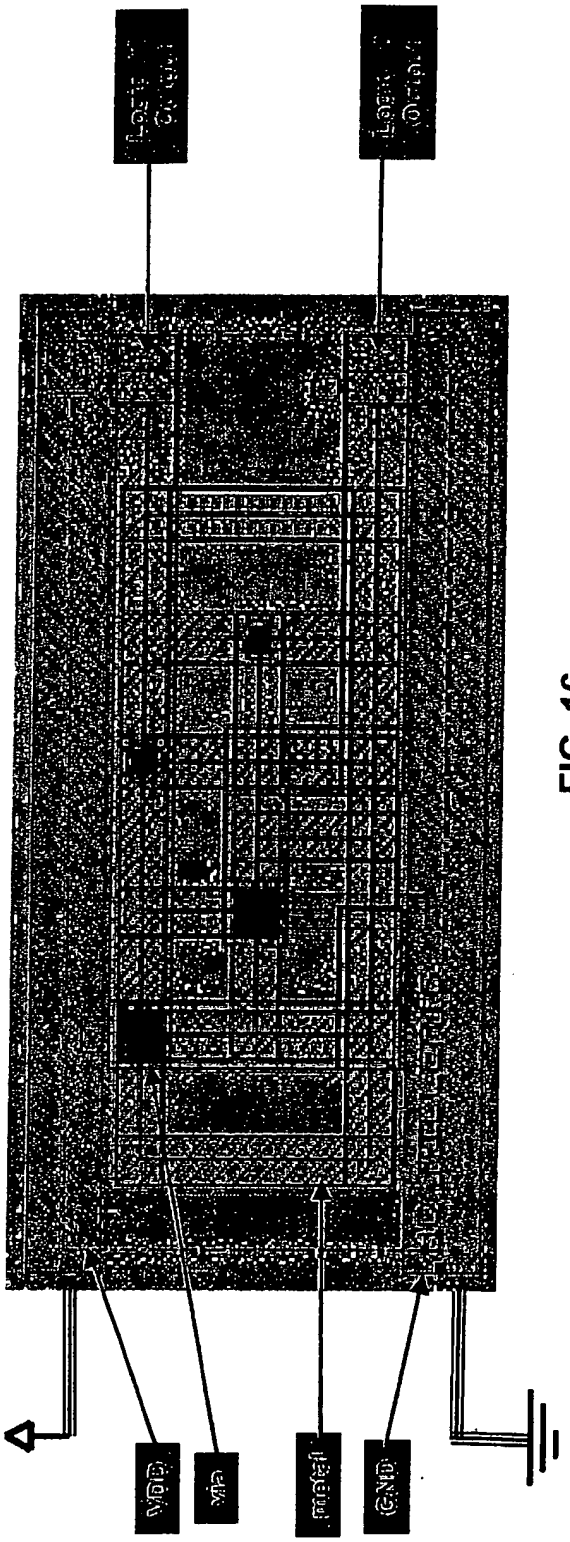


FIG. 16

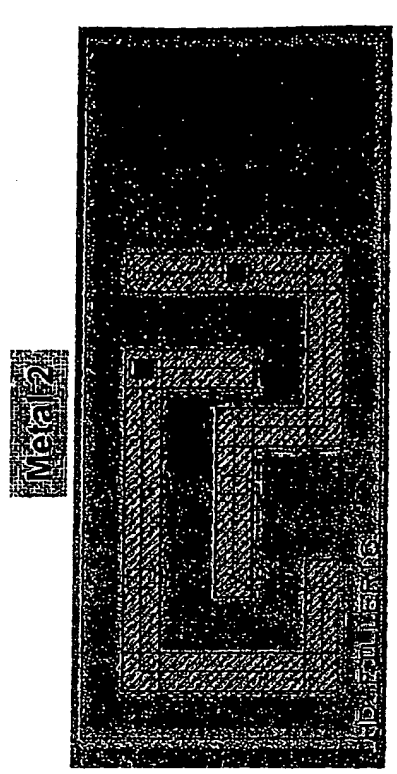


FIG. 17B

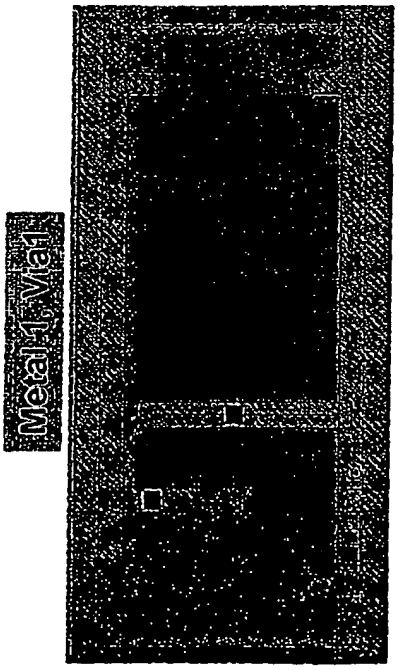


FIG. 17A

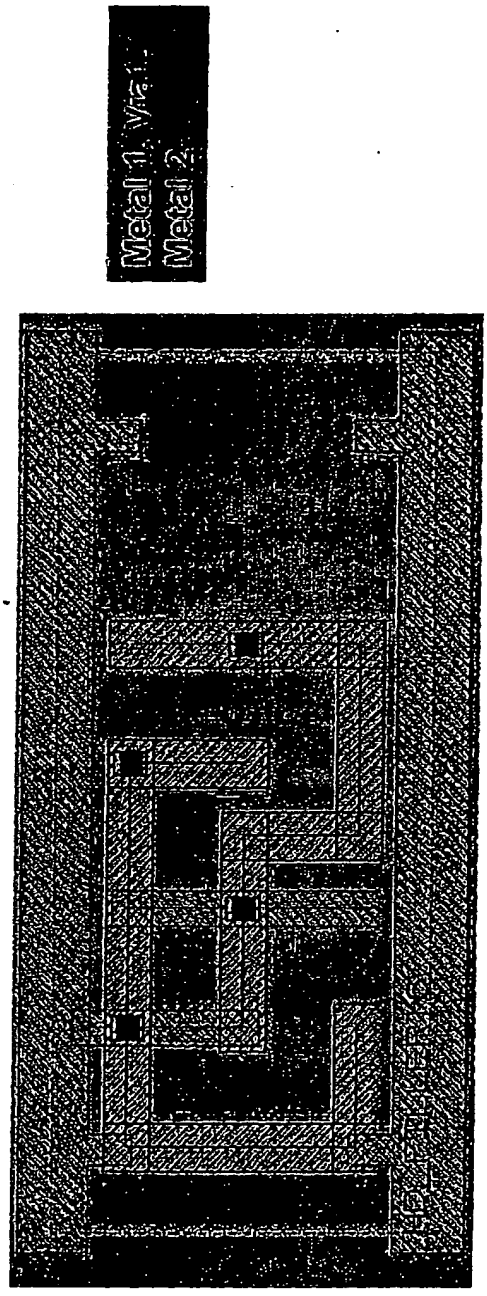


FIG. 17C

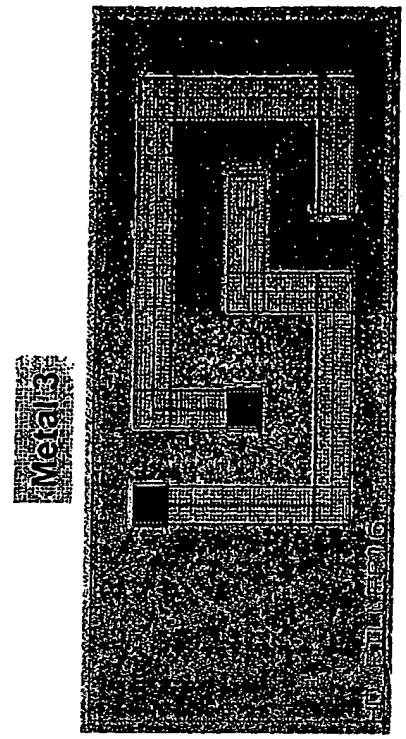


FIG. 18B

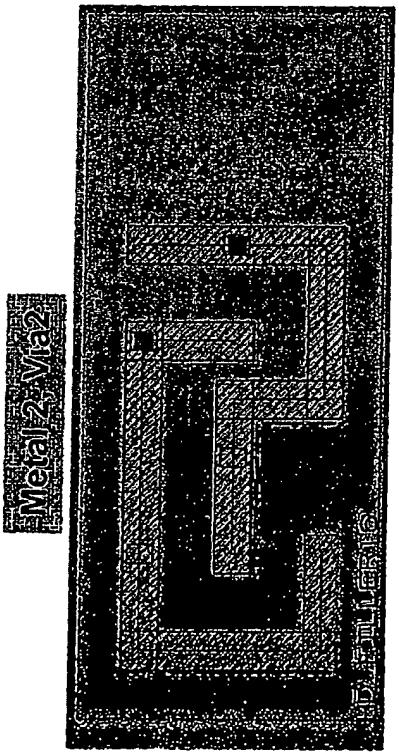


FIG. 18A

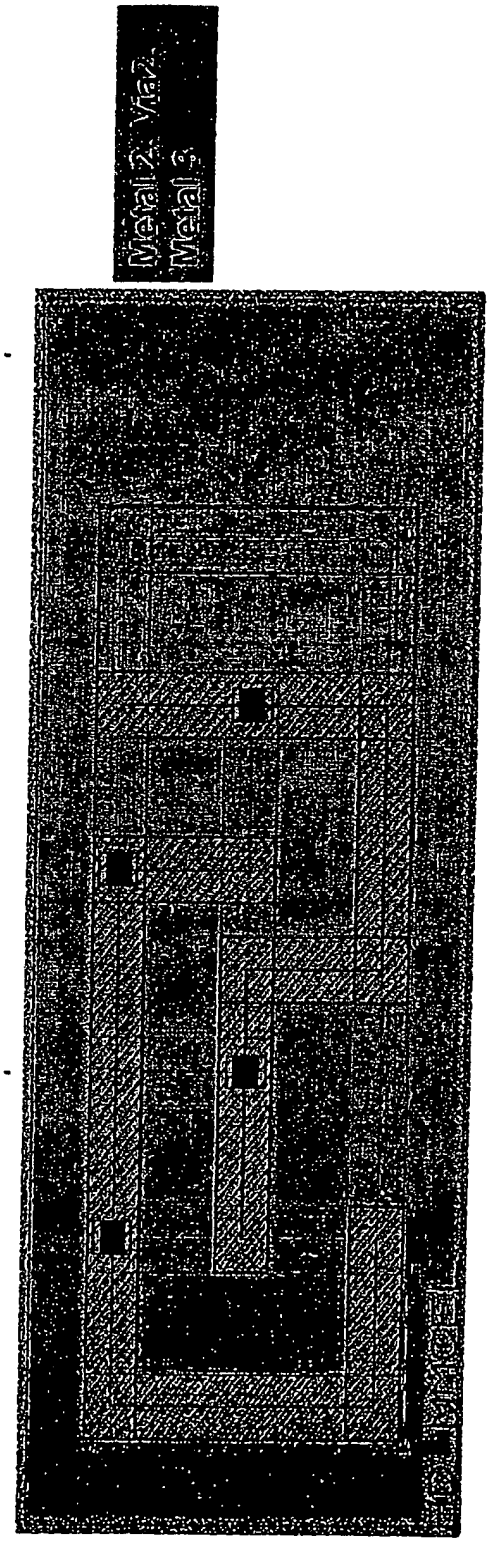


FIG. 18C

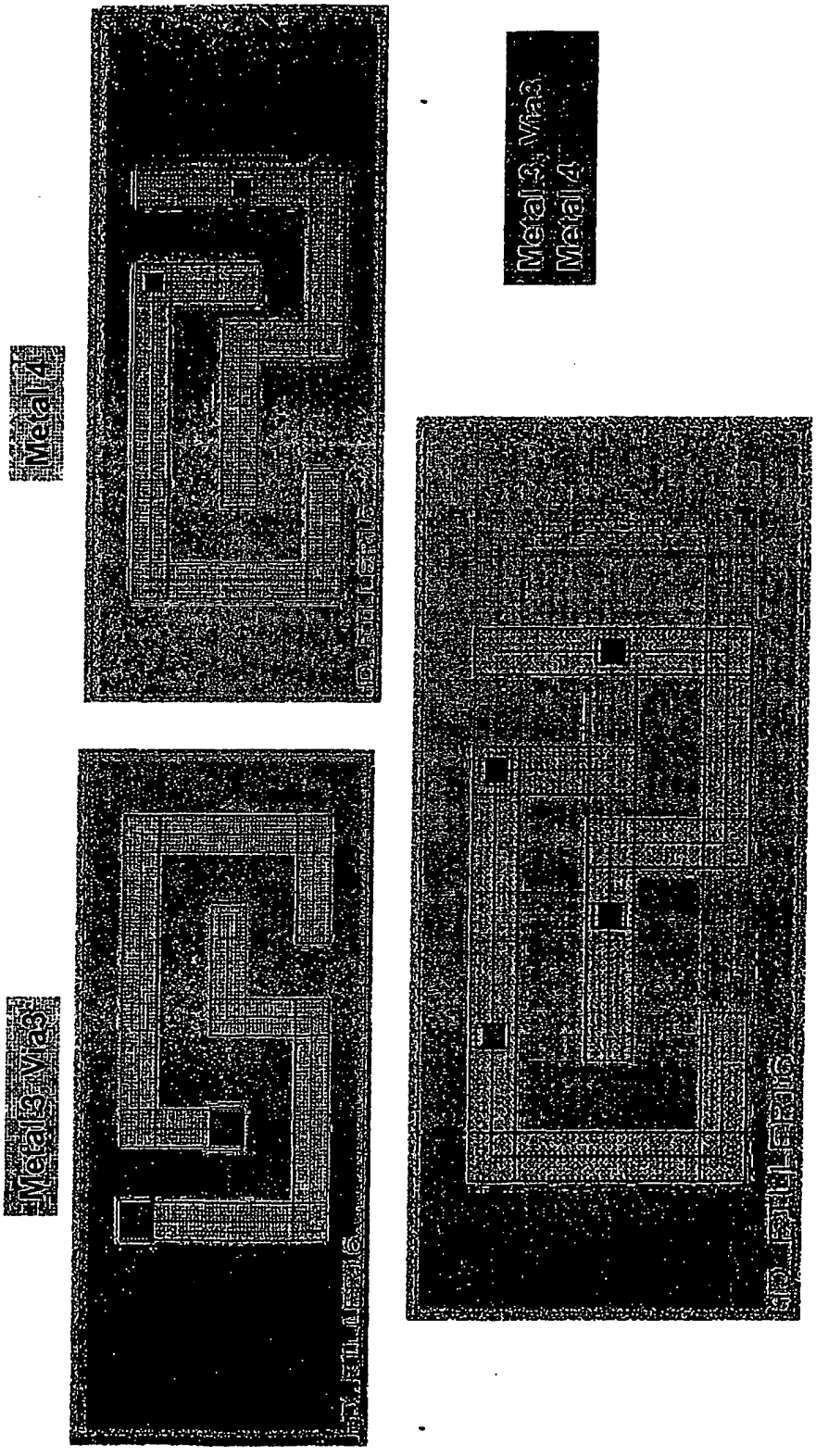


FIG. 19A

FIG. 19B

FIG. 19C

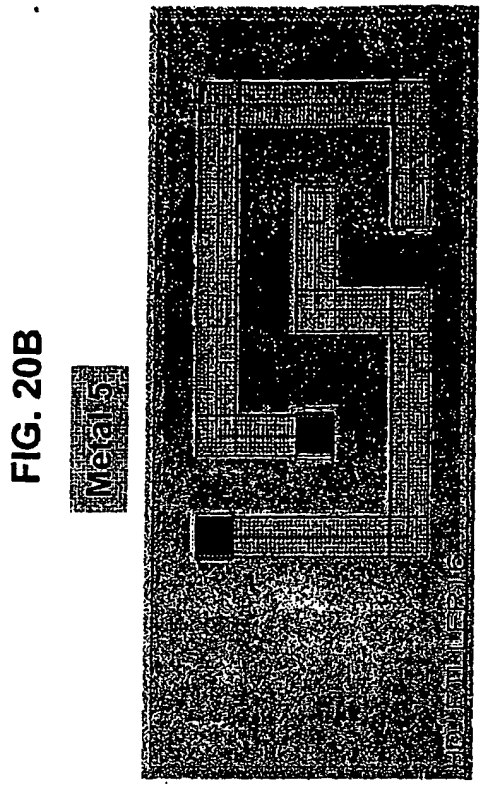


FIG. 20B

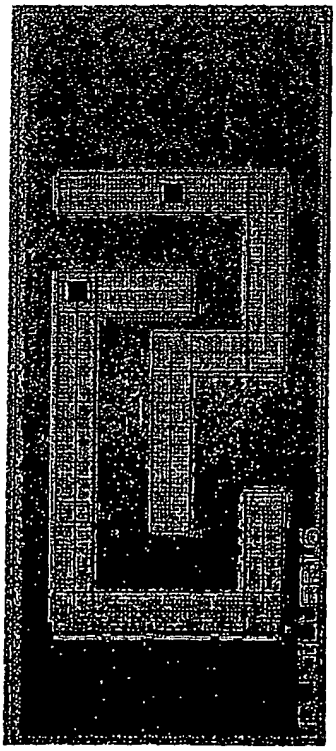


FIG. 20A

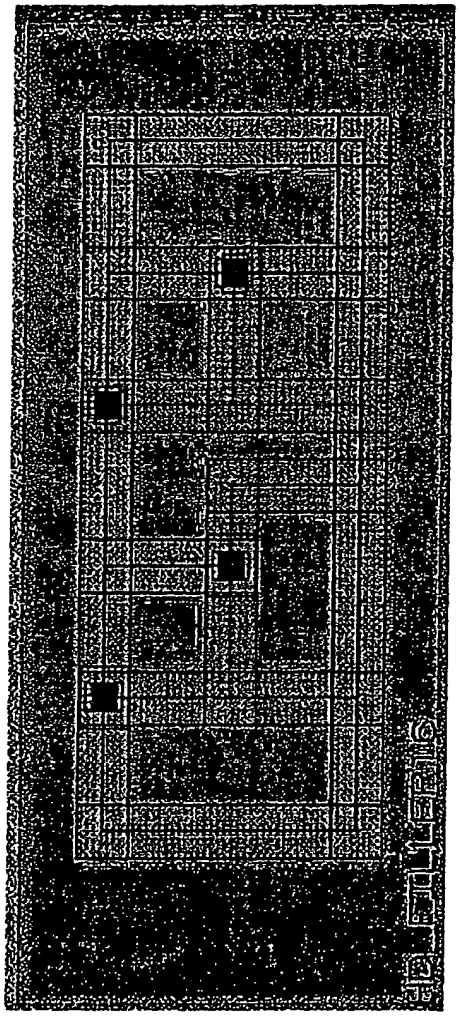


FIG. 20C

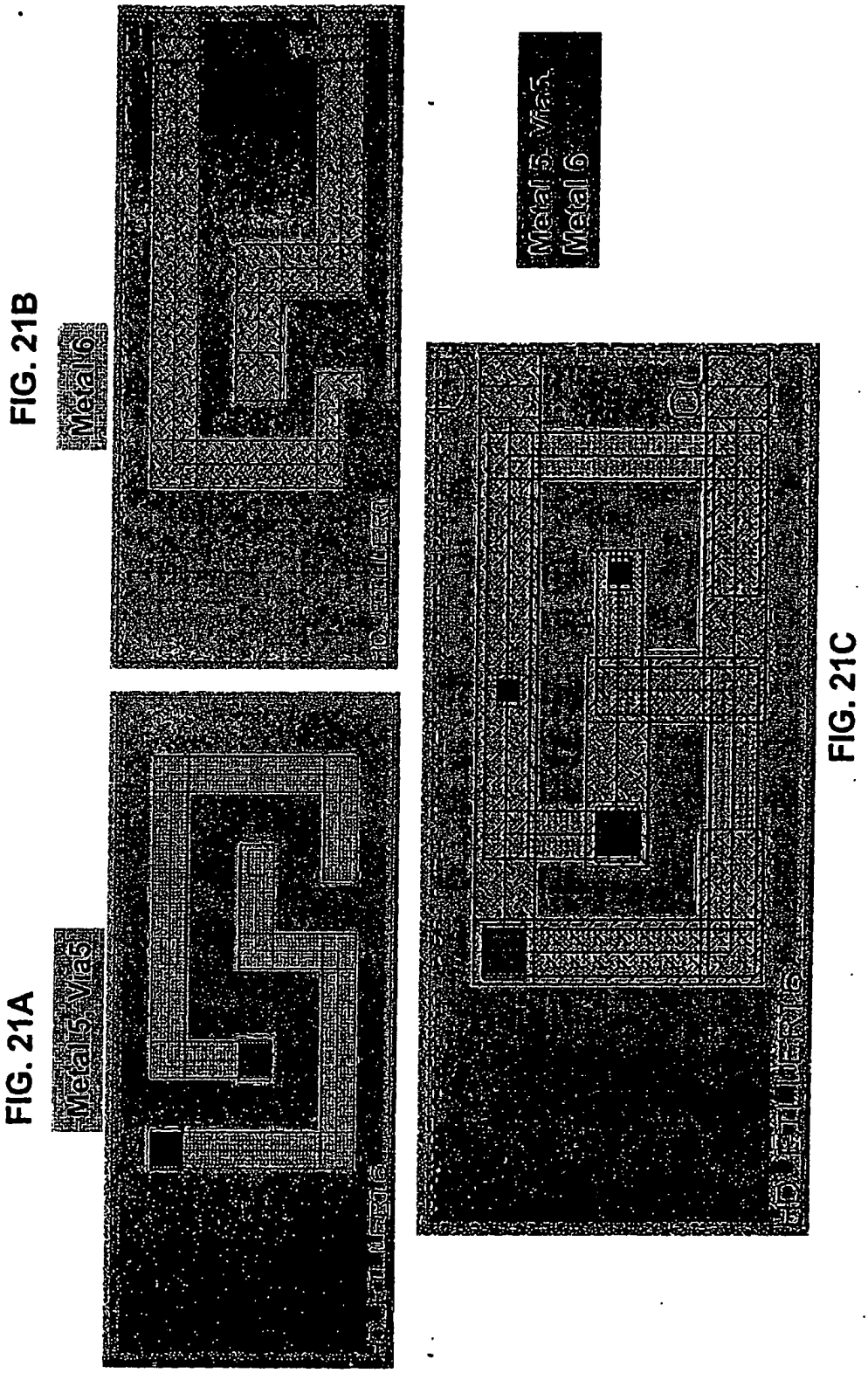


FIG. 21A

FIG. 21B

FIG. 21C

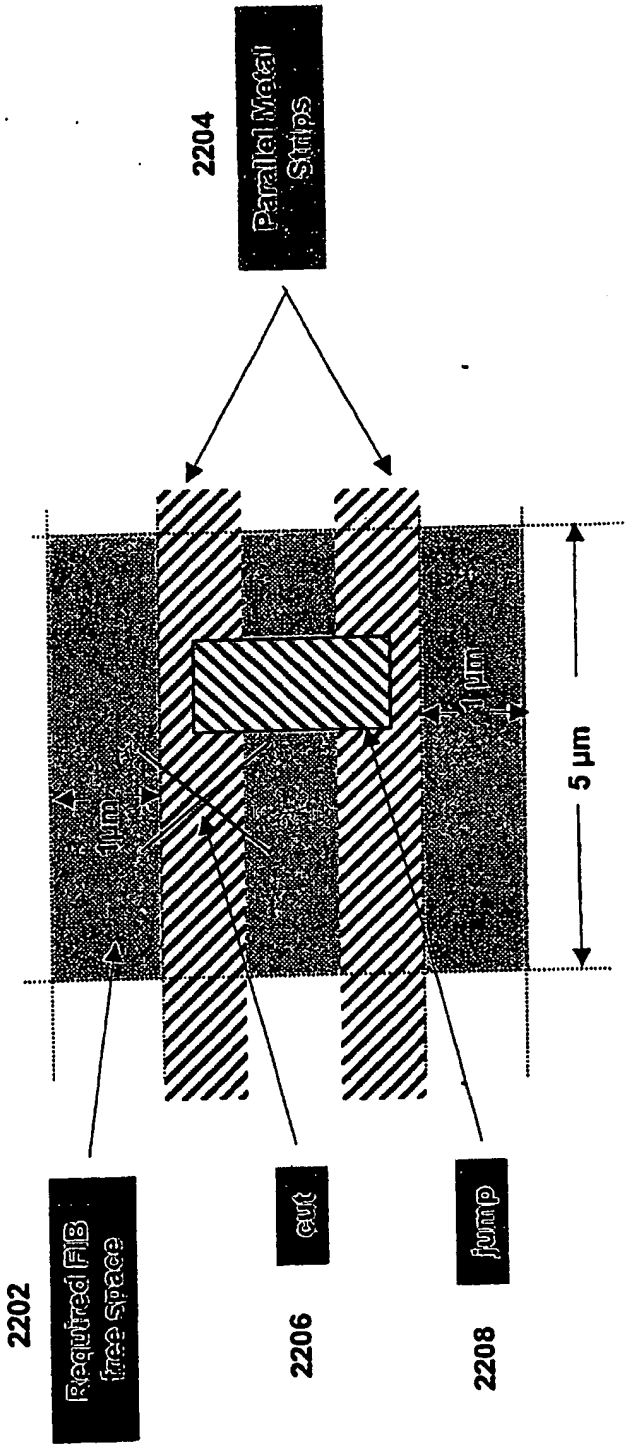

2204
Parallel Metal Strips
1 µm
1 µm
5 µm
2202
Required FIB free Space
cut
2206
jump
2208

FIG. 22

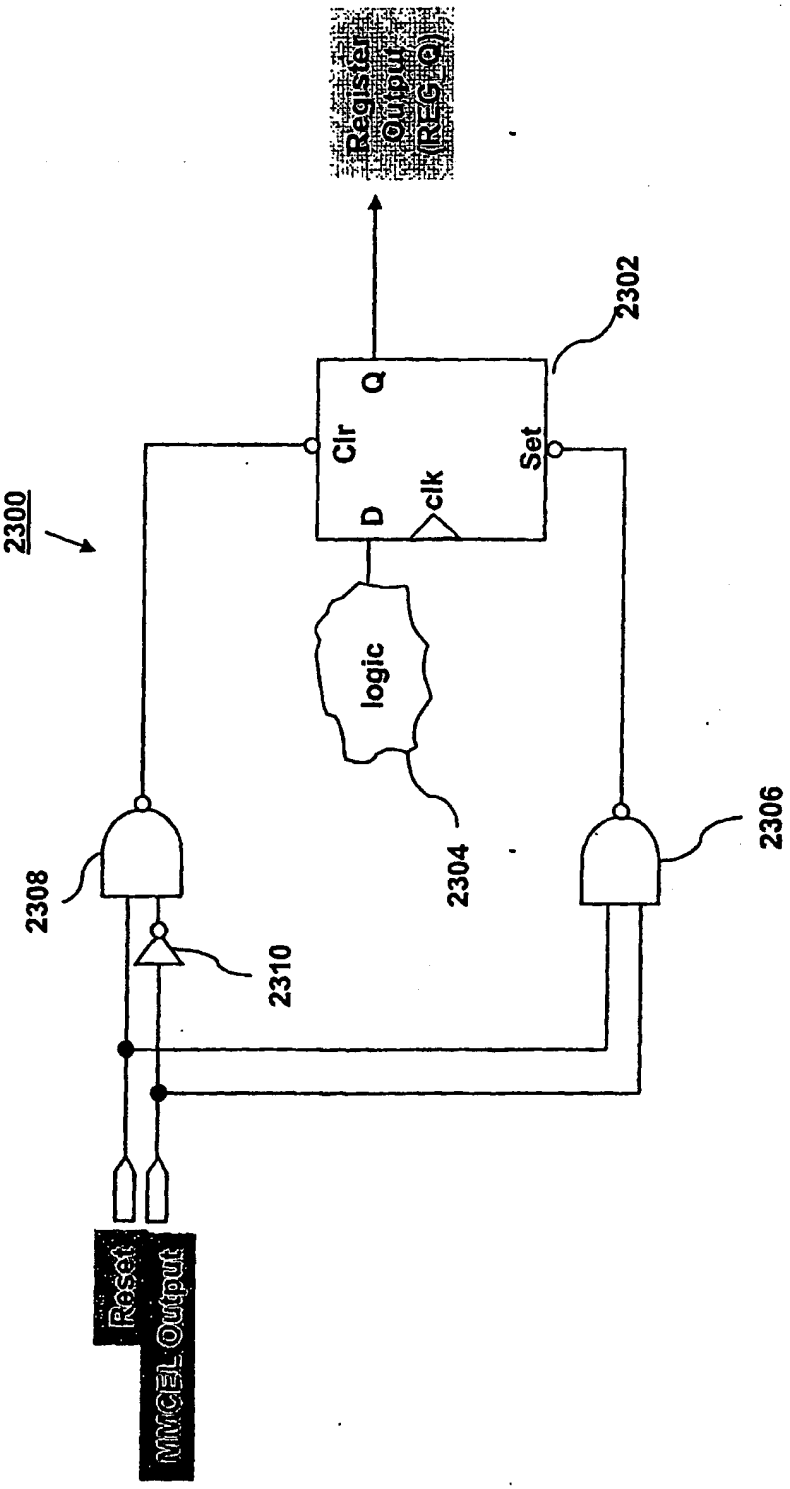

Register Output (REG Q)
2302
Q
Clr
Set
D
clk
2300
logic
2304
2306
2308
2310
Reset
NMOSEL Output

FIG. 23

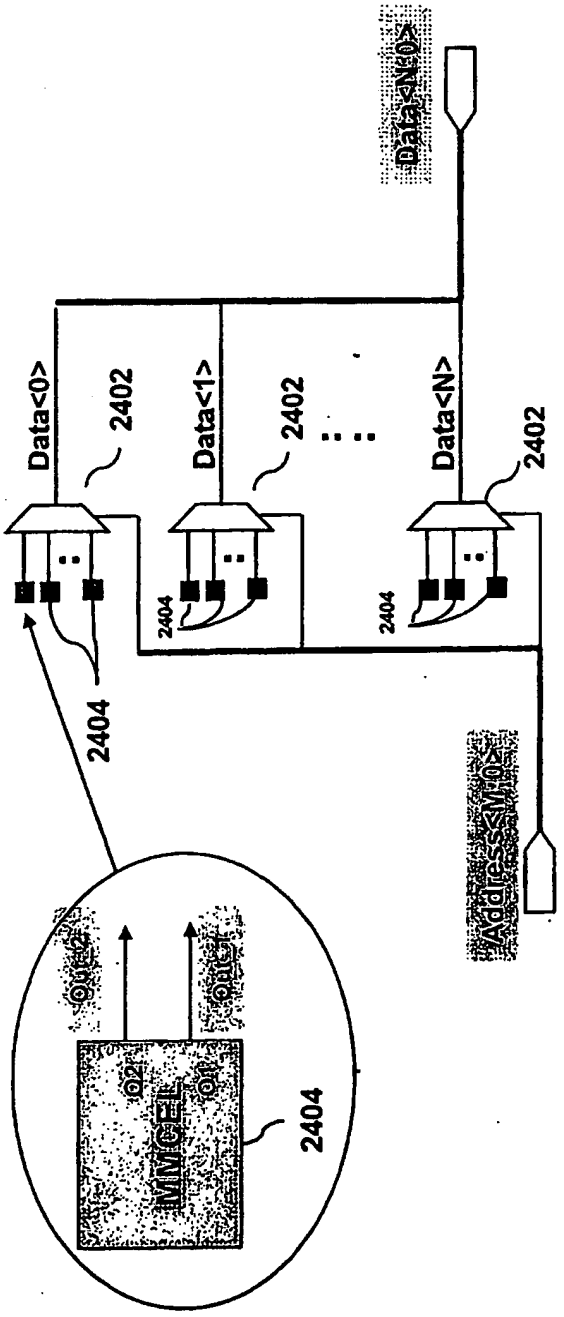

Data<N:0>
Data<0>
2402
Data<1>
2402
Data<N>
2402
2404
2404
2404
2404
Address<M:0>
out2
out1
MMCEL
2404

FIG. 24

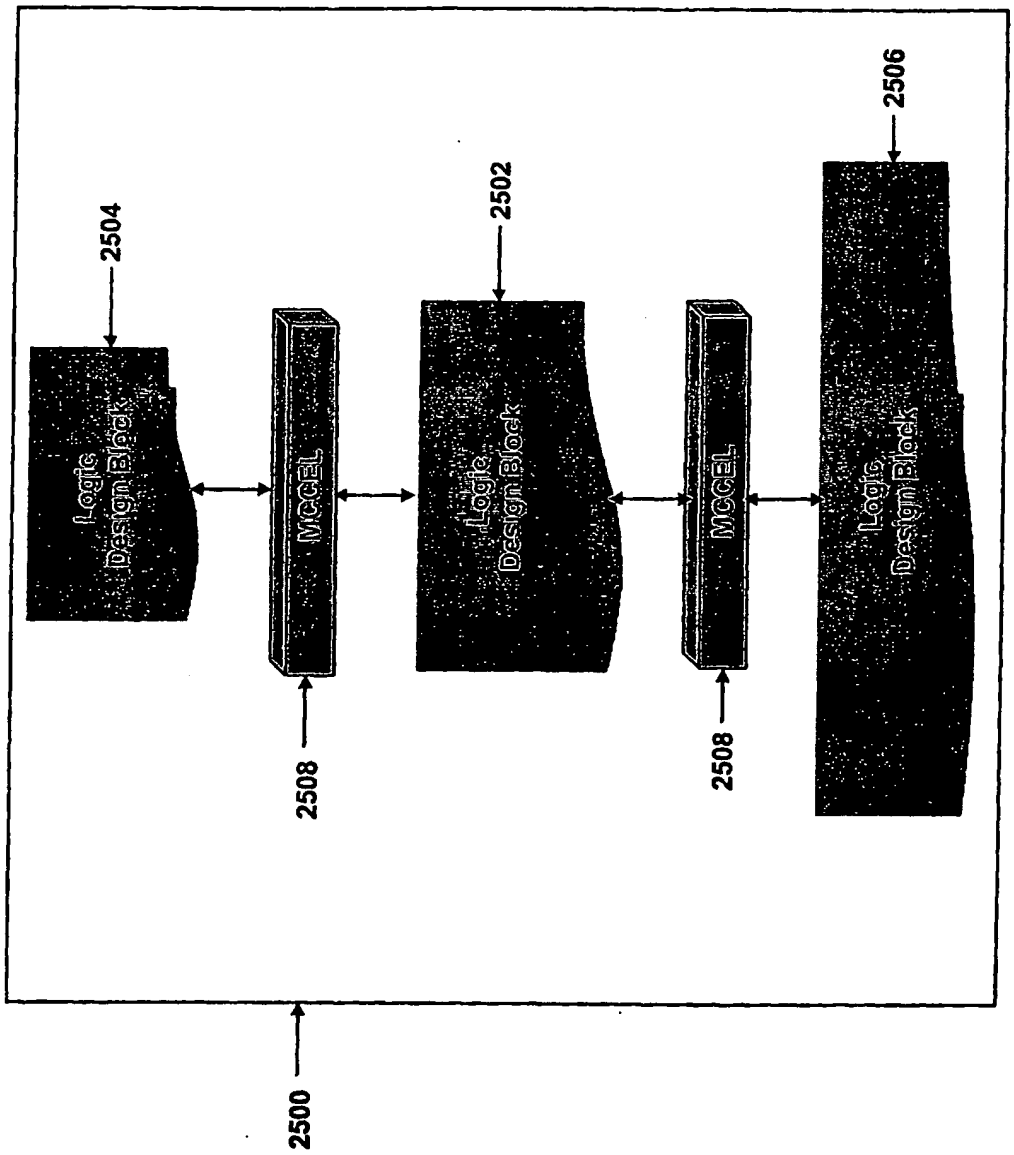

2500
2504
Logic Design Block
MCCEL
2508
2502
Logic Design Block
MCCEL
2508
2506
Logic Design Block

FIG. 25

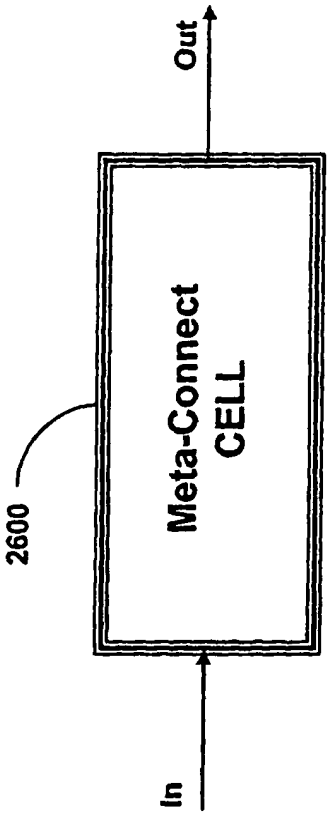


FIG. 26A

Out	Comment
In	Default Connect at any layer
0	Tied to GND at any layer
1	Tied to VDD at any layer

FIG. 26B

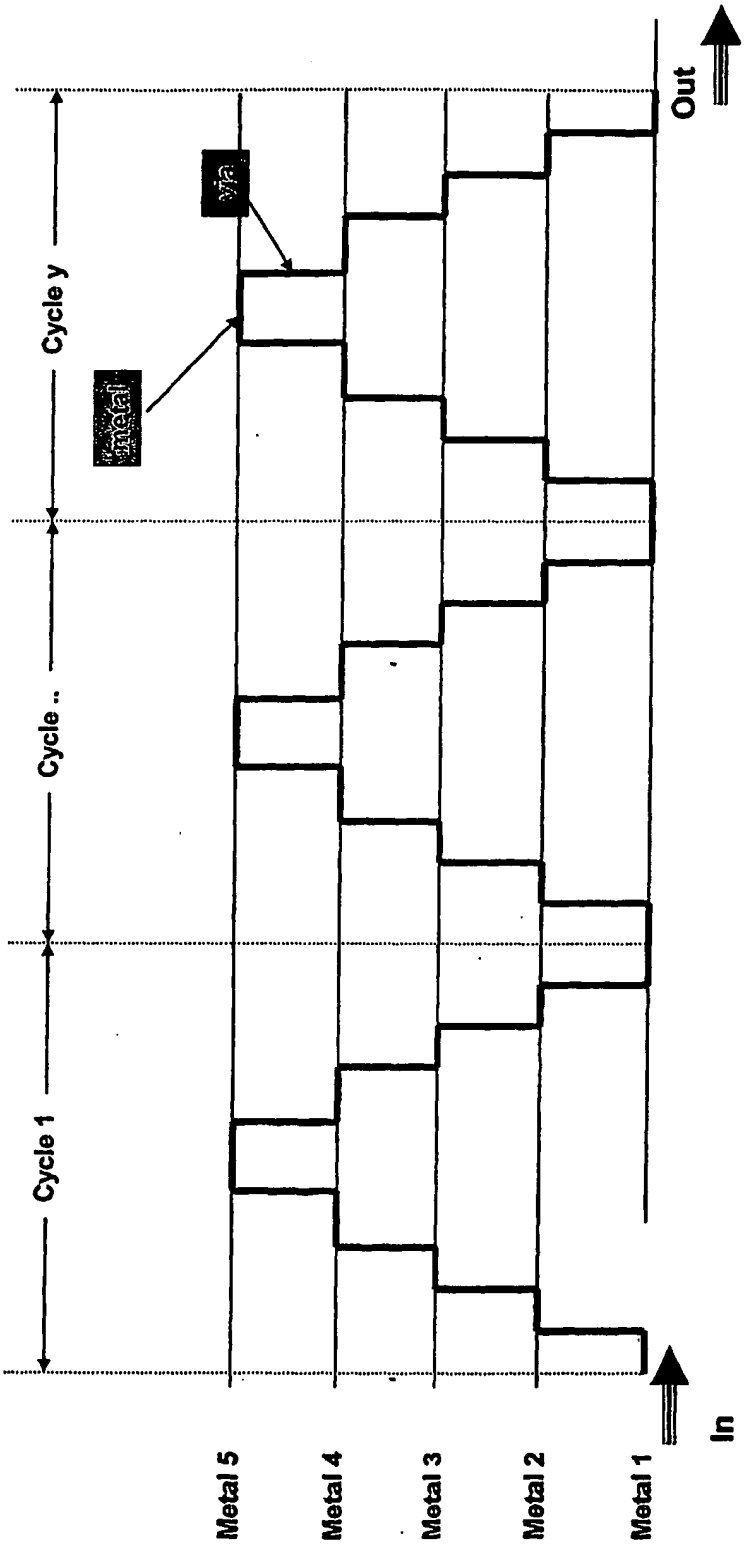

Out
Via
Metal
Cycle y
Cycle ..
Cycle 1
In
Metal 5
Metal 4
Metal 3
Metal 2
Metal 1

FIG. 27

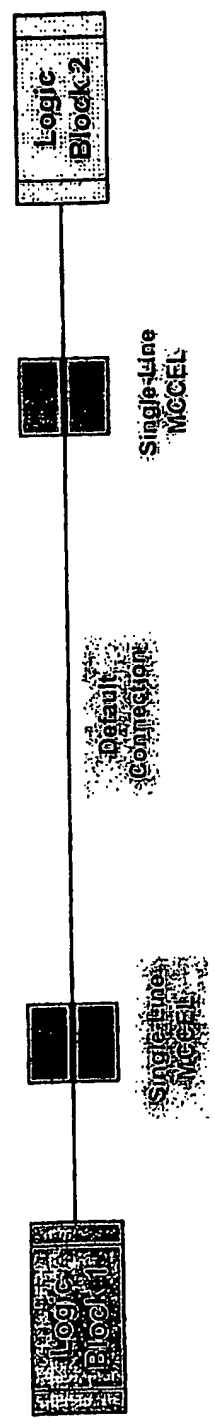


FIG. 28A

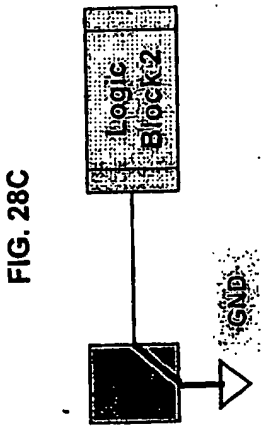


FIG. 28C

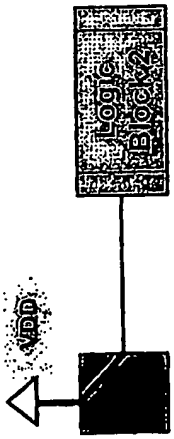


FIG. 28B

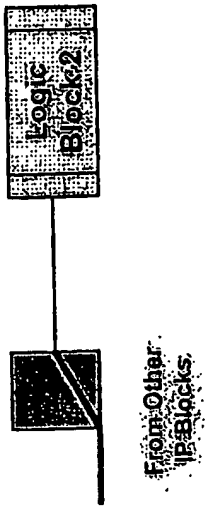


FIG. 28D

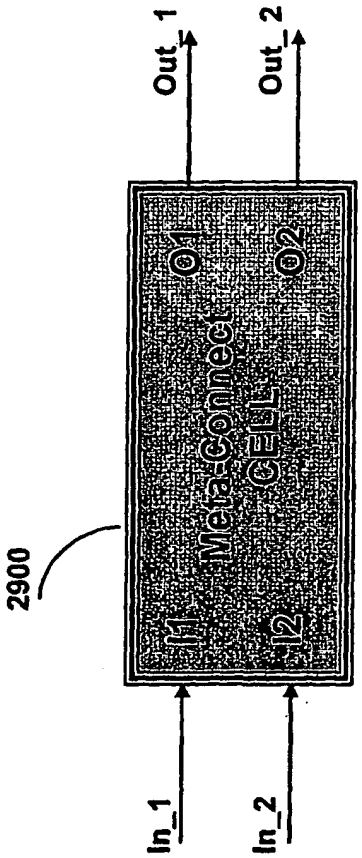


FIG. 29A

Toggle	Out_1	Out_2	Comment
0	In_1	In_2	Default
1	In_2	In_1	Metal/Via Change

FIG. 29B

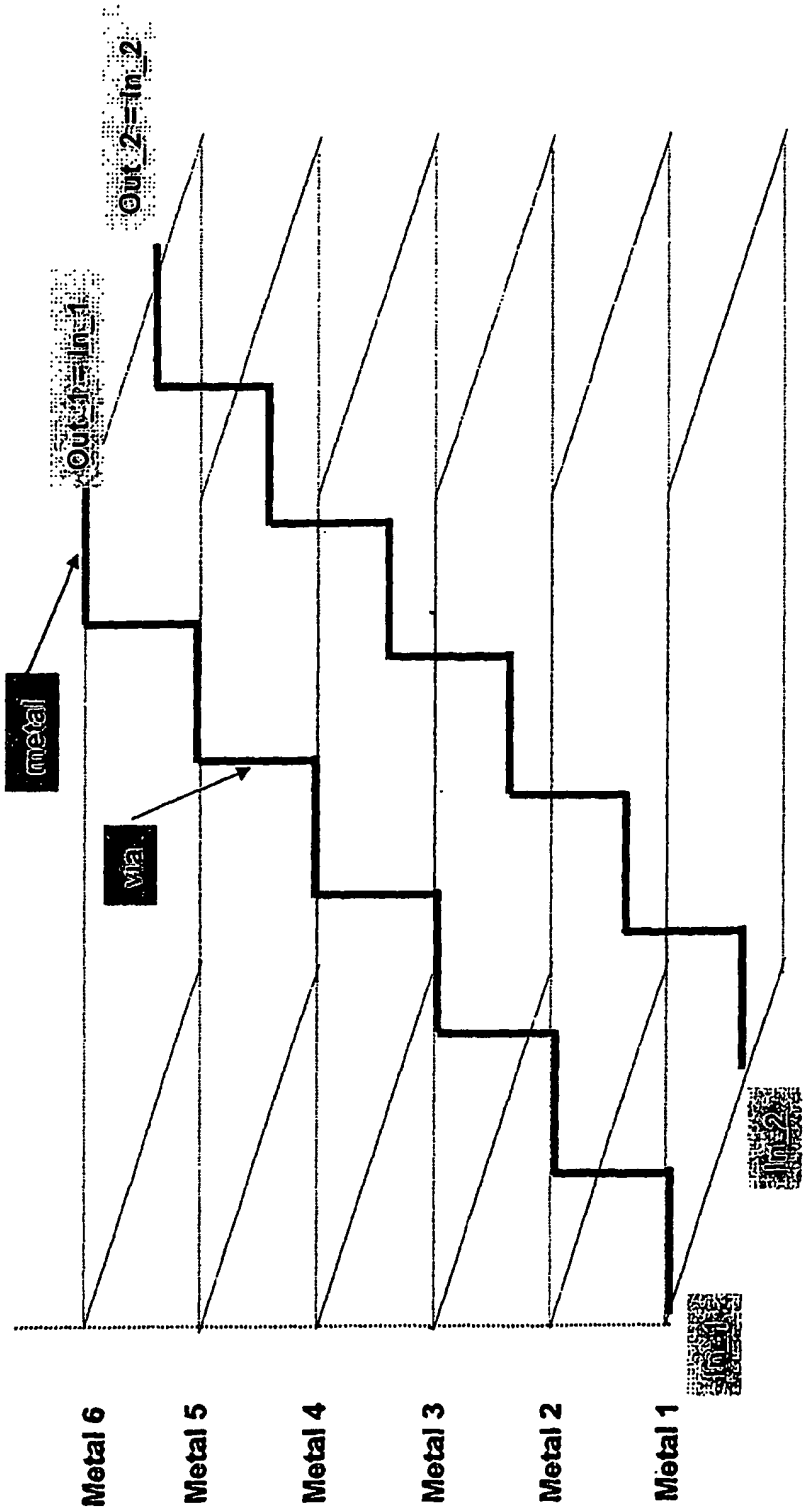


FIG. 30

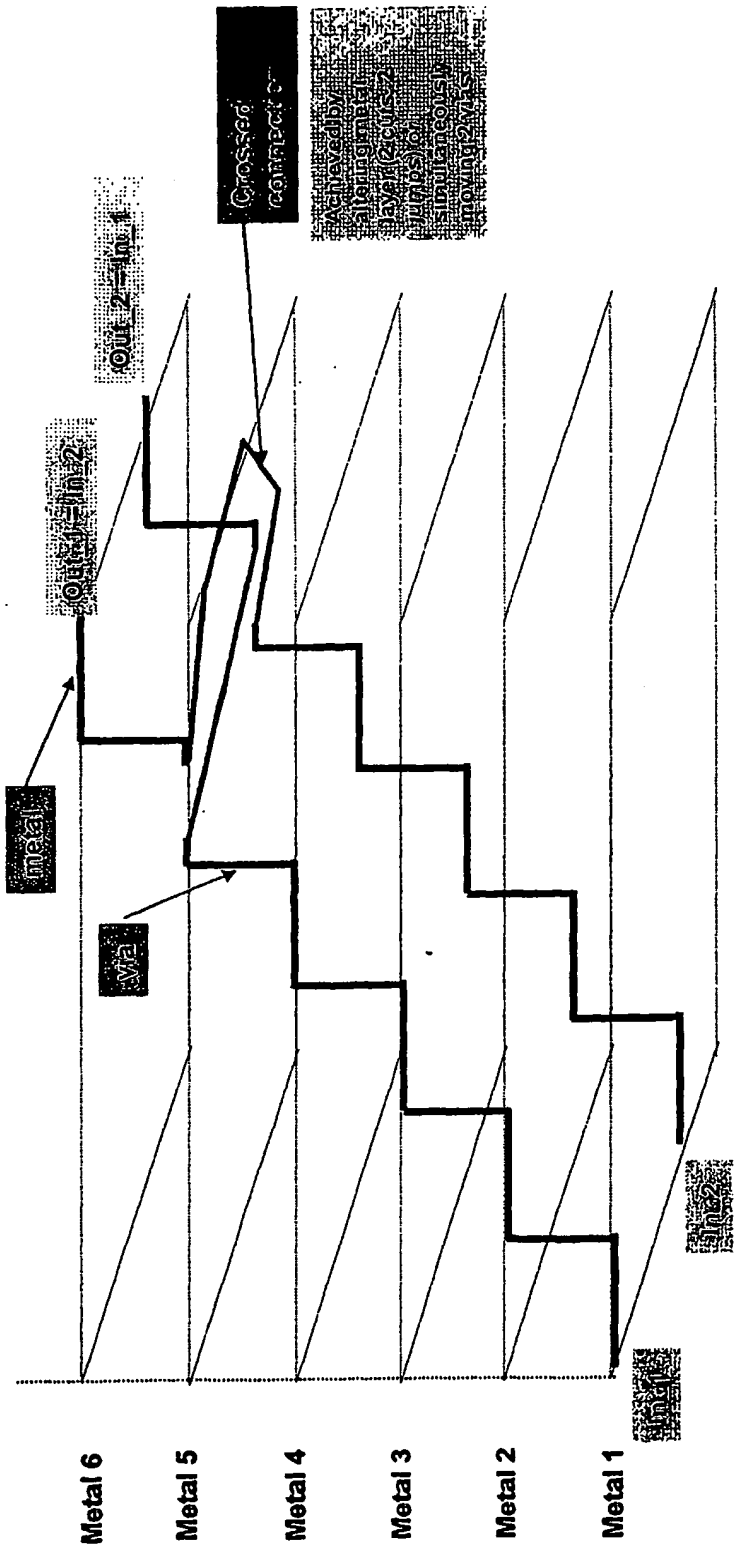


FIG. 31

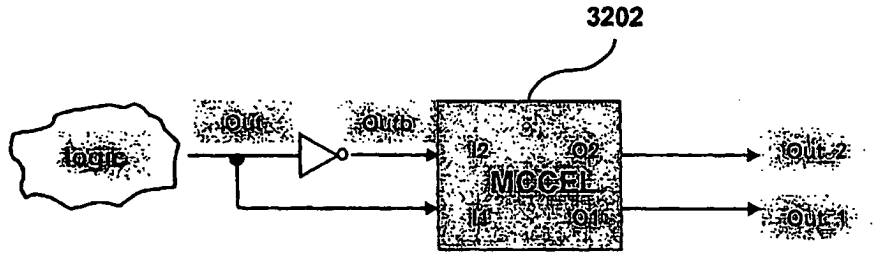


FIG. 32A

Out_1	Out_2	Comment
Out	Outb	Default
Outb	Out	Metal/Via Change

FIG. 32B

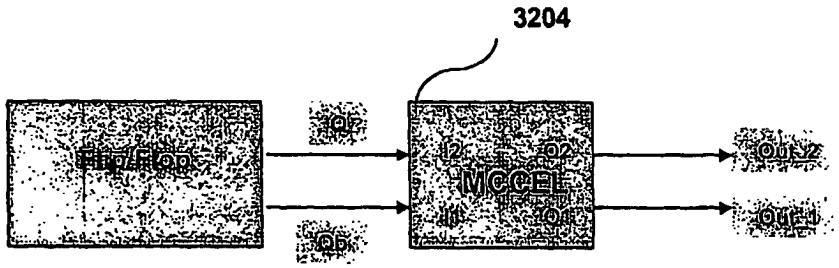


FIG. 32C

Out_1	Out_2	Comment
Q	Qb	Default
Qb	Q	Metal/Via Change

FIG. 32D

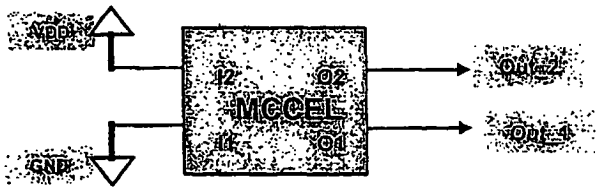


FIG. 33A

Out_1	Out_2	Comment
0	1	Default
1	0	Metal/Via Change

FIG. 33B

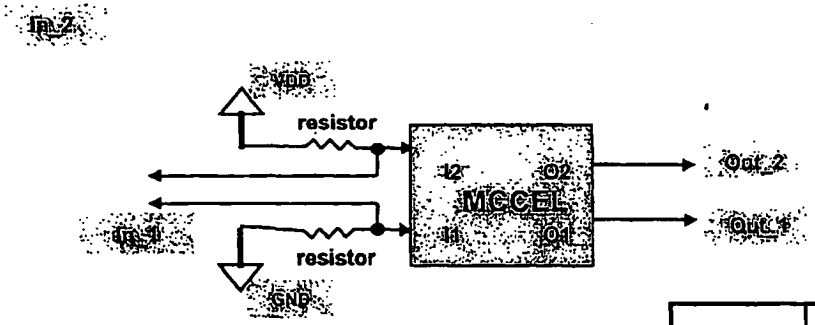


FIG. 33C

Out_1	Out_2	Comment
weak '0'	weak '1'	Default (In_1 & In_2 floating)
weak '1'	weak '0'	Metal/Via Change (In_1 & In_2 floating)
In_1	In_2	Default (In_1 & In_2 driven)
In_2	In_1	Metal/Via Change (In_1 & In_2 driven)

FIG. 33D

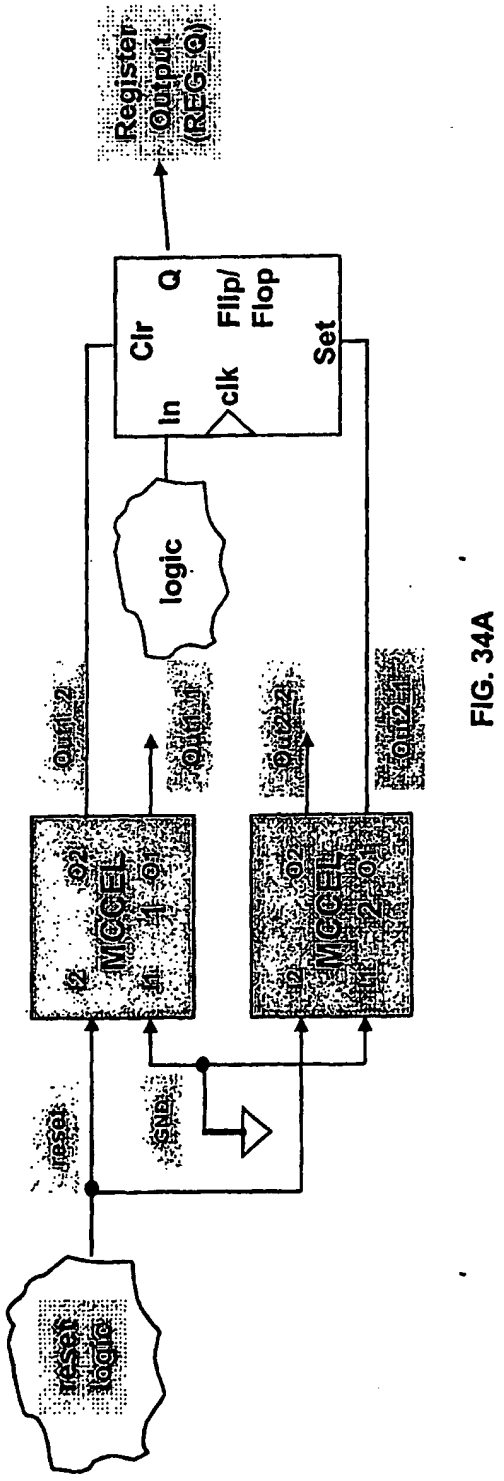


FIG. 34A

Reset	MCCEL 1	MCCEL 2	Reg_Q
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	X
1	0	1	X
1	1	0	X
1	1	1	1

FIG. 34B

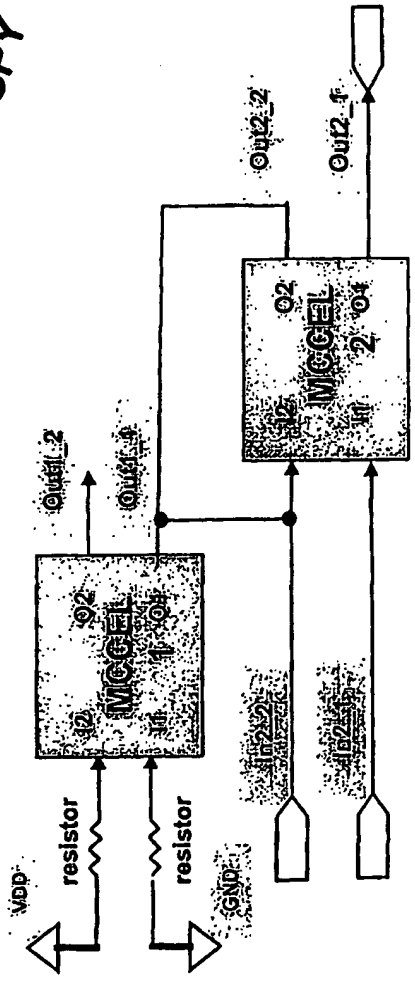


FIG. 35A

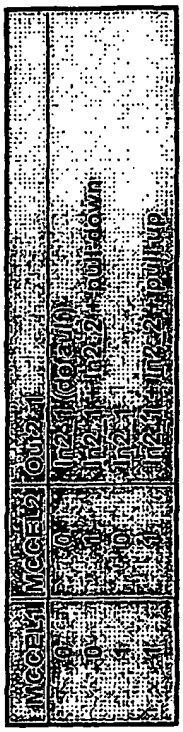


FIG. 35B

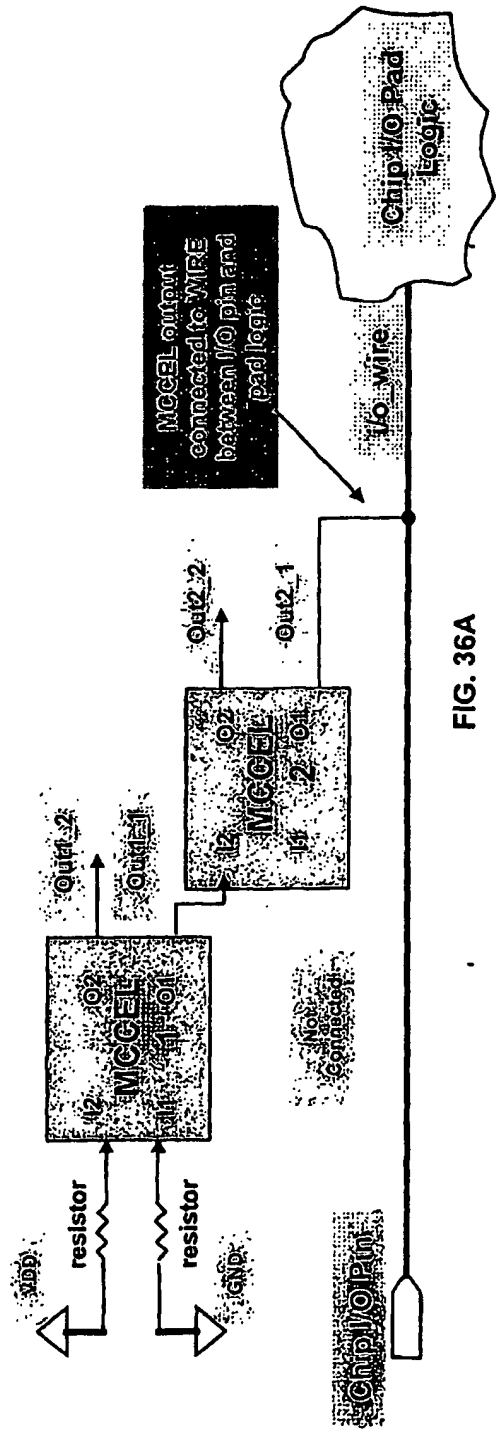


FIG. 36A

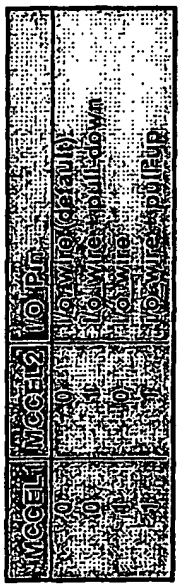


FIG. 36B

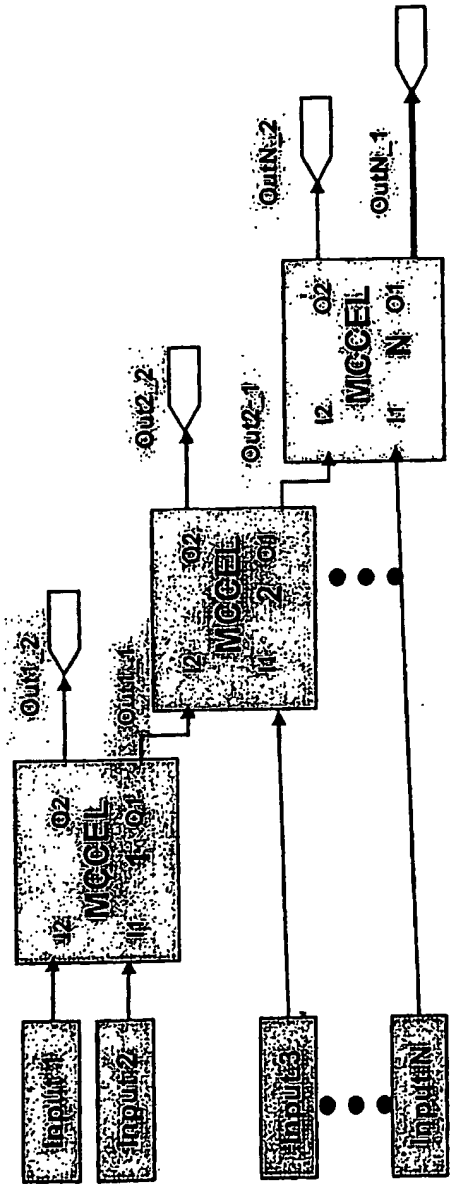

Input1
Input2
Input3
InputN
MCCEL 1-1
MCCEL 2-1
MCCEL N-1
Out1_2
Out1_1
Out2_2
Out2_1
OutN_2
OutN_1

FIG. 37

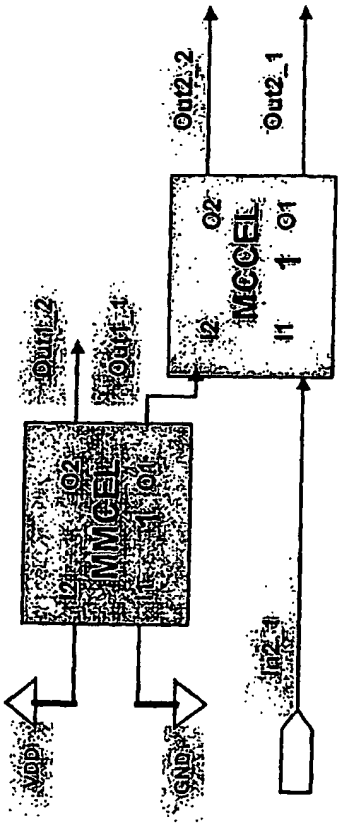


FIG. 38A

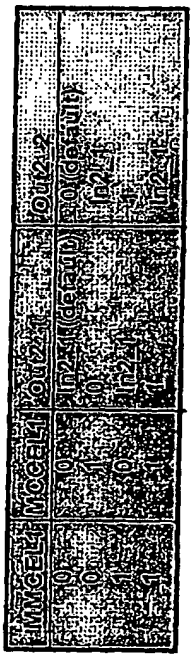


FIG. 38B

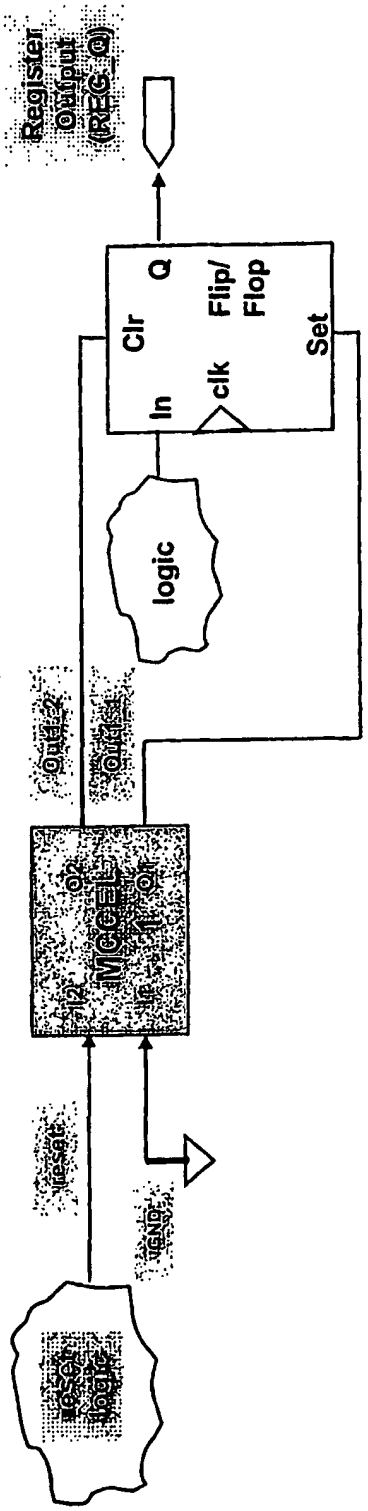


FIG. 39A

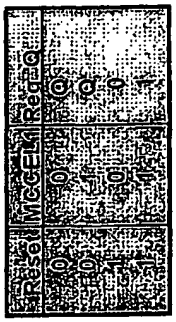


FIG. 39B

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 04 01 3796

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
X	GB 2 338 593 A (TEXAS INSTRUMENTS LTD) 22 December 1999 (1999-12-22) * the whole document *	1-8	H01L23/544 H01L23/525 H01L23/528 H01L23/58 G06F11/00 G11C17/10
X	US 5 408 428 A (BURGESS BRADLEY ET AL) 18 April 1995 (1995-04-18) * the whole document *	4,5,8	
X	US 6 292 024 B1 (JENSEN RUNE HARTUNG ET AL) 18 September 2001 (2001-09-18) * abstract; figure 3 *	1-3,6,7	
X	EP 1 100 125 A (ST MICROELECTRONICS SRL) 16 May 2001 (2001-05-16) * the whole document *	1-3,6,7	
A	US 5 459 355 A (KREIFELS JERRY A) 17 October 1995 (1995-10-17) * the whole document *	1-8	

TECHNICAL FIELDS SEARCHED (Int.Cl.7)
H01L
G06F
G11C

~~The present search report has been drawn up for all claims~~

Place of search	Date of completion of the search	Examiner
Munich	13 October 2004	Kuchenbecker, J

CATEGORY OF CITED DOCUMENTS
X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

European Patent Office

Application Number
EP 04 01 3796

CLAIMS INCURRING FEES

The present European patent application comprised at the time of filing more than ten claims.

☐ Only part of the claims have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims and for those claims for which claims fees have been paid, namely claim(s):

☐ No claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims.

LACK OF UNITY OF INVENTION

The Search Division considers that the present European patent application does not comply with the requirements of unity of invention and relates to several inventions or groups of inventions, namely:

see sheet B

☐ All further search fees have been paid within the fixed time limit. The present European search report has been drawn up for all claims.

☐ As all searchable claims could be searched without effort justifying an additional fee, the Search Division did not invite payment of any additional fee.

☐ Only part of the further search fees have been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the inventions in respect of which search fees have been paid, namely claims:

☒ None of the further search fees have been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the invention first mentioned in the claims, namely claims:

1-8

European Patent Office

LACK OF UNITY OF INVENTION
SHEET B

Application Number
EP 04 01 3796

The Search Division considers that the present European patent application does not comply with the requirements of unity of invention and relates to several inventions or groups of inventions, namely:

1. claims: 1-8

An integrated circuit chip including a plurality of metal layers and first and second supply potentials, a programmable memory cell for storing a value, the memory cell comprising:
*a first metal interconnect structure that traverses the plurality of metal layers using a first plurality of vias;
*a second metal interconnect structure that traverses the plurality of metal layers using a second plurality of vias; and
*at least one output coupled to one of the first and second supply potentials by at least one of said first and second metal interconnect structures, wherein a state of said at least one output is programmable by altering at least one of the plurality of metal layers.

---

2. claim: 9

A programmable memory cell circuit for modification of a default regsister value comprising:
* a first metal interconnect structure traversing a plurality of metal layers,
* a second metal interconnect structure traversing a plurality of metal layers,
* an output wherein the state of said output is programmable by altering at least one of the plurality of metal layers;
* a register having a data input, a data output and control inputs,
* a control circuit coupled to the control inputs of the register.

---

3. claim: 10

An integrated circuit chip including at least two adjacent logic blocks comprising:
* a first metal interconnect structure traversing a plurality of metal layers,
* a second metal interconnect structure traversing a plurality of metal layers,
* an interconnect formed between said adjacent blocks by at least one of said first and second metal interconnect structures wherein said interconnect is programmable by altering any one of the plurality of metal layers.

ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 04 01 3796

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

13-10-2004

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
GB 2338593 A	22-12-1999	NONE	
US 5408428 A	18-04-1995	NONE	
US 6292024 B1	18-09-2001	WO 0145170 A1	21-06-2001
		EP 1155451 A1	21-11-2001
		JP 2003517213 T	20-05-2003
		US 2001011909 A1	09-08-2001
EP 1100125 A	16-05-2001	EP 1100125 A1	16-05-2001
US 5459355 A	17-10-1995	NONE	

EPO FORM P0459

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82